Virtual Memory

Daniel Sanchez
Computer Science & Artificial Intelligence Lab
M.I.T.
Reminder: Operating Systems

- Goals of OS:

  - process_1
  - ... process_N

  Operating system

  Hardware
Reminder: Operating Systems

- Goals of OS:
  - Protection and privacy: Processes cannot access each other’s data
Reminder: Operating Systems

- Goals of OS:
  - Protection and privacy: Processes cannot access each other’s data
  - Abstraction: Hide away details of underlying hardware
• **Goals of OS:**
  - Protection and privacy: Processes cannot access each other’s data
  - Abstraction: Hide away details of underlying hardware
    • e.g., processes open and access files instead of issuing raw commands to hard drive
Reminder: Operating Systems

• Goals of OS:
  – Protection and privacy: Processes cannot access each other’s data
  – Abstraction: Hide away details of underlying hardware
    • e.g., processes open and access files instead of issuing raw commands to hard drive
  – Resource management: Controls how processes share hardware resources (CPU, memory, disk, etc.)
Reminder: Operating Systems

• Goals of OS:
  – Protection and privacy: Processes cannot access each other’s data
  – Abstraction: Hide away details of underlying hardware
    • e.g., processes open and access files instead of issuing raw commands to hard drive
  – Resource management: Controls how processes share hardware resources (CPU, memory, disk, etc.)

• Key enabling technologies:
Reminder: Operating Systems

• Goals of OS:
  – Protection and privacy: Processes cannot access each other’s data
  – Abstraction: Hide away details of underlying hardware
    • e.g., processes open and access files instead of issuing raw commands to hard drive
  – Resource management: Controls how processes share hardware resources (CPU, memory, disk, etc.)

• Key enabling technologies:
  – User mode + supervisor mode
  – Interrupts to safely transition into supervisor mode
Reminder: Operating Systems

• Goals of OS:
  – Protection and privacy: Processes cannot access each other’s data
  – Abstraction: Hide away details of underlying hardware
    • e.g., processes open and access files instead of issuing raw commands to hard drive
  – Resource management: Controls how processes share hardware resources (CPU, memory, disk, etc.)

• Key enabling technologies:
  – User mode + supervisor mode
  – Interrupts to safely transition into supervisor mode

process\_1 \ldots process\_N

Operating system

Hardware

April 12, 2018
Reminder: Operating Systems

• Goals of OS:
  – Protection and privacy: Processes cannot access each other’s data
  – Abstraction: Hide away details of underlying hardware
    • e.g., processes open and access files instead of issuing raw commands to hard drive
  – Resource management: Controls how processes share hardware resources (CPU, memory, disk, etc.)

• Key enabling technologies:
  – User mode + supervisor mode
  – Interrupts to safely transition into supervisor mode
  – Virtual memory to abstract the storage resources of the machine

April 12, 2018
• **Goals of OS:**
  - Protection and privacy: Processes cannot access each other’s data
  - Abstraction: Hide away details of underlying hardware
    • e.g., processes open and access files instead of issuing raw commands to hard drive
  - Resource management: Controls how processes share hardware resources (CPU, memory, disk, etc.)

• **Key enabling technologies:**
  - User mode + supervisor mode
  - Interrupts to safely transition into supervisor mode
  - Virtual memory to abstract the storage resources of the machine
Virtual Memory (VM) Systems

*Illusion of a large, private, uniform store*

- Protection & Privacy
  - Each process has a private address space
Virtual Memory (VM) Systems

*Illusion of a large, private, uniform store*

- **Protection & Privacy**
  - Each process has a private address space

- **Demand Paging**
  - Provides the ability to run programs larger than main memory
  - Hides differences in machine configuration
Virtual Memory (VM) Systems
*Illusion of a large, private, uniform store*

- **Protection & Privacy**
  - Each process has a private address space

- **Demand Paging**
  - Provides the ability to run programs larger than main memory
  - Hides differences in machine configuration

The price of VM is address translation on each memory reference
Names for Memory Locations

- Machine language address
  - As specified in machine code
- Virtual address
  - ISA specifies translation of machine code address into virtual address of program variable (sometime called effective address)
- Physical address
  - Operating system specifies mapping of virtual address into name for a physical memory location
Names for Memory Locations

- **Machine language address**
  - As specified in machine code

- **Virtual address**
  - ISA specifies translation of machine code address into virtual address of program variable (sometime called *effective address*)

- **Physical address**
  - Operating system specifies mapping of virtual address into name for a physical memory location
Segmentation (Base-and-Bound) Address Translation

Process Address Space

0x0 to 0x0fff

Physical Memory

0x0 to 0xf..ff

April 12, 2018
• Each program’s data is allocated in a contiguous segment of physical memory.
Each program’s data is allocated in a contiguous segment of physical memory.
Each program’s data is allocated in a contiguous segment of physical memory.

Physical address = Virtual Address + Segment Base.
Each program’s data is allocated in a contiguous segment of physical memory.
Physical address = Virtual Address + Segment Base
Bound register provides safety and isolation.
Segmentation (Base-and-Bound) Address Translation

- Each program’s data is allocated in a contiguous segment of physical memory
- Physical address = Virtual Address + Segment Base
- Bound register provides safety and isolation
- Base and Bound registers should not be accessed by user programs (only accessible in supervisor mode)
Separate Segments for Code and Data

Load X

Program Address Space

Main Memory

data segment

code segment

Virtual Address

Data Base Register

Data Bound Register

Code Base Register

Program Counter

Code Bound Register

\[ \text{Virtual Address} \leq \text{Data Bound Register} \rightarrow \text{Main Memory} \]

\[ \text{Virtual Address} + \text{Data Base Register} \rightarrow \text{Main Memory} \]

\[ \text{Virtual Address} \leq \text{Code Bound Register} \rightarrow \text{Main Memory} \]

\[ \text{Virtual Address} + \text{Code Base Register} \rightarrow \text{Main Memory} \]

Bounds Violation?

 Bounds Violation?
Separate Segments for Code and Data

Pros of this separation?
Separate Segments for Code and Data

Pros of this separation?
Prevents buggy program from overwriting code
Separate Segments for Code and Data

Pros of this separation?

Prevents buggy program from overwriting code

Multiple processes can share code segment
Memory Fragmentation

OS Space

- proc 1: 16K
- proc 2: 24K
- proc 2: 24K
- proc 3: 32K
- proc 3: 24K

free
Memory Fragmentation

Processes 4 & 5 start

OS Space

proc 1
16K

proc 2
24K
24K

proc 3
32K
24K

free
Memory Fragmentation

Processes 4 & 5 start

OS Space

proc 1
16K
proc 2
24K
proc 3
24K
32K
24K
proc 4
16K
proc 5
proc 3
32K
proc 4
8K
proc 5
24K

OS Space

proc 1
16K
proc 2
24K
proc 3
proc 4
16K
proc 5
24K

free
Memory Fragmentation

Processes 4 & 5 start
- proc 1: 16K
- proc 2: 24K
- proc 3: 24K
- proc 4: 32K

Processes 2 & 5 end
- proc 1: 16K
- proc 2: 24K
- proc 4: 16K
- proc 3: 8K
- proc 5: 24K

Free space
Memory Fragmentation

Processes 4 & 5 start

Processes 2 & 5 end

L16-7
As processes start and end, storage is “fragmented”. Therefore, at some point segments have to be moved around to compact the free space.

April 12, 2018
Paged Memory Systems

- Divide physical memory in fixed-size blocks called **pages**
  - Typical page size: 4KB
Paged Memory Systems

- Divide physical memory in fixed-size blocks called **pages**
  - Typical page size: 4KB

- Interpret each virtual address as a pair
  `<virtual page number, offset>`
Paged Memory Systems

- Divide physical memory in fixed-size blocks called pages
  - Typical page size: 4KB

- Interpret each virtual address as a pair <virtual page number, offset>

- Use a page table to translate from virtual to physical page numbers
  - Page table contains the physical page number (i.e., starting physical address) for each virtual page number
Each process has a page table
Page table has an entry for each process page
Private Address Space per Process

- Each process has a page table
- Page table has an entry for each process page

*Page tables make it possible to store the pages of a program non-contiguously*
Paging vs. Segmentation

Pros of paging vs segmentation?
Paging vs. Segmentation

Pros of paging vs segmentation?

Paging avoids fragmentation issues
Paging vs. Segmentation

Pros of paging vs segmentation?

Paging avoids fragmentation issues

Paging allows programs that use more virtual memory than the machine’s physical memory (demand paging)
Paging vs. Segmentation

Pros of paging vs segmentation?

Paging avoids fragmentation issues

Paging allows programs that use more virtual memory than the machine’s physical memory (demand paging)

Cons of paging vs segmentation?
Paging vs. Segmentation

Pros of paging vs segmentation?

Paging avoids fragmentation issues

Paging allows programs that use more virtual memory than the machine’s physical memory (demand paging)

Cons of paging vs segmentation?

Page tables are MUCH larger than base & bound regs!
Paging vs. Segmentation

Pros of paging vs segmentation?

Paging avoids fragmentation issues

Paging allows programs that use more virtual memory than the machine’s physical memory (demand paging)

Cons of paging vs segmentation?

Page tables are MUCH larger than base & bound regs!

...where do we store the page tables?
Suppose Page Tables reside in memory.
Suppose Page Tables reside in memory

Virtual Page Number

VPN  offset

PT Base Reg

System PT Base

System PT

PT Proc 1

PT Proc 2

PTB Proc i
Suppose Page Tables reside in memory
Suppose Page Tables reside in memory

Virtual Page Number

VPN offset

PT Base Reg

System PT Base

PT Proc 1

PT Proc 2

System PT

Physical Page Number

PTB Proc $i$

Virtual Page Number

Physical Page Number

Virtual Page Number

VPN offset

PT Base Reg

System PT Base

PT Proc 1

PT Proc 2

System PT

Physical Page Number

PTB Proc $i$
Suppose Page Tables reside in memory

Virtual Page Number

VPN | offset

PT Base Reg

System PT Base

PT Proc 1

PT Proc 2

System PT

Physical Page Number

PTB Proc $i$
Suppose Page Tables reside in memory
Suppose Page Tables reside in memory

Translation:
- PPN = Mem[PT Base + VPN]
- PA = PPN + offset
Suppose Page Tables reside in memory

- Translation:
  - \( \text{PPN} = \text{Mem}[\text{PT Base} + \text{VPN}] \)
  - \( \text{PA} = \text{PPN} + \text{offset} \)

- All links represent physical addresses; no VA to PA translation
Suppose Page Tables reside in memory

- Translation:
  - PPN = Mem[PT Base + VPN]
  - PA = PPN + offset
- All links represent physical addresses; no VA to PA translation
- On process switch
  - PT Base Reg := System PT Base + new process ID
Suppose Page Tables reside in memory

- Translation:
  - $\text{PPN} = \text{Mem}[\text{PT Base} + \text{VPN}]$
  - $\text{PA} = \text{PPN} + \text{offset}$

- All links represent physical addresses; no VA to PA translation

- On process switch
  - $\text{PT Base Reg} := \text{System PT Base} + \text{new process ID}$

Accessing one data word or instruction requires two DRAM accesses!
Paging Implementation Issues

- How to reduce memory access overhead
  - A good VM design must be fast and space-efficient

- What if all the pages can’t fit in DRAM?
Paging Implementation Issues

- How to reduce memory access overhead
  - A good VM design must be fast and space-efficient

- What if all the pages can’t fit in DRAM?
  - What if the process page table can’t fit in DRAM?
Paging Implementation Issues

• How to reduce memory access overhead
  – A good VM design must be fast and space-efficient

• What if all the pages can’t fit in DRAM?
  – What if the process page table can’t fit in DRAM?
  – What if the System page table can’t fit in DRAM?
Paging Implementation Issues

• How to reduce memory access overhead
  – A good VM design must be fast and space-efficient

• What if all the pages can’t fit in DRAM?
  – What if the process page table can’t fit in DRAM?
  – What if the System page table can’t fit in DRAM?

Beyond the scope of this subject
Demand Paging

Using main memory as a cache of disk

- All the pages of the processes may not fit in main memory. Therefore, DRAM is backed up by swap space on disk.
- Page Table Entry (PTE) contains:
Demand Paging
Using main memory as a cache of disk

- All the pages of the processes may not fit in main memory. Therefore, DRAM is backed up by swap space on disk.
- Page Table Entry (PTE) contains:
Demand Paging

Using main memory as a cache of disk

- All the pages of the processes may not fit in main memory. Therefore, DRAM is backed up by swap space on disk.
- Page Table Entry (PTE) contains:
  - A resident bit to indicate if the page exists in main memory
Demand Paging
*Using main memory as a cache of disk*

- All the pages of the processes may not fit in main memory. Therefore, DRAM is backed up by *swap space* on disk.
- Page Table Entry (PTE) contains:
  - A *resident* bit to indicate if the page exists in main memory
  - PPN (physical page number) for a memory-resident page
Demand Paging

Using main memory as a cache of disk

- All the pages of the processes may not fit in main memory. Therefore, DRAM is backed up by swap space on disk.
- Page Table Entry (PTE) contains:
  - A **resident** bit to indicate if the page exists in main memory
  - **PPN** (physical page number) for a memory-resident page
  - **DPN** (disk page number) for a page on the disk
Demand Paging

Using main memory as a cache of disk

- All the pages of the processes may not fit in main memory. Therefore, DRAM is backed up by swap space on disk.

- Page Table Entry (PTE) contains:
  - A resident bit to indicate if the page exists in main memory
  - PPN (physical page number) for a memory-resident page
  - DPN (disk page number) for a page on the disk
  - Protection and usage bits
Demand Paging
Using main memory as a cache of disk

- All the pages of the processes may not fit in main memory. Therefore, DRAM is backed up by swap space on disk.
- Page Table Entry (PTE) contains:
  - A resident bit to indicate if the page exists in main memory
  - PPN (physical page number) for a memory-resident page
  - DPN (disk page number) for a page on the disk
  - Protection and usage bits
- Even if all pages fit in memory, demand paging allows bringing only what is needed from disk
Demand Paging
Using main memory as a cache of disk

- All the pages of the processes may not fit in main memory. Therefore, DRAM is backed up by swap space on disk.
- Page Table Entry (PTE) contains:
  - A resident bit to indicate if the page exists in main memory
  - PPN (physical page number) for a memory-resident page
  - DPN (disk page number) for a page on the disk
  - Protection and usage bits
- Even if all pages fit in memory, demand paging allows bringing only what is needed from disk
  - When a process starts, all code and data are on disk; bring pages in as they are accessed
Example: Virtual → Physical Translation

Setup:
- 256 bytes/page ($2^8$)
- 16 virtual pages ($2^4$)
- 8 physical pages ($2^3$)
- 12-bit VA (4 vpn, 8 offset)
- 11-bit PA (3 ppn, 8 offset)

lw 0x2C8(x0)
VA = 0x2C8, PA = _______
Example: Virtual → Physical Translation

16-entry Page Table

<table>
<thead>
<tr>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>5</td>
<td>6</td>
<td>7</td>
</tr>
<tr>
<td>8</td>
<td>9</td>
<td>A</td>
<td>B</td>
</tr>
<tr>
<td>C</td>
<td>D</td>
<td>E</td>
<td>F</td>
</tr>
</tbody>
</table>


- VPN 0x4
- VPN 0x5
- VPN 0x0
- VPN 0xF
- VPN 0x2
- VPN 0xE
- VPN 0xDD
- VPN 0xC

Setup:
- 256 bytes/page (2^8)
- 16 virtual pages (2^4)
- 8 physical pages (2^3)
- 12-bit VA (4 vpn, 8 offset)
- 11-bit PA (3 ppn, 8 offset)

lw 0x2C8(x0)
VA = 0x2C8, PA = ________
Example: Virtual → Physical Translation

Setup:
- 256 bytes/page ($2^8$)
- 16 virtual pages ($2^4$)
- 8 physical pages ($2^3$)
- 12-bit VA (4 vpn, 8 offset)
- 11-bit PA (3 ppn, 8 offset)

lw 0x2C8(x0)
VA = 0x2C8, PA = ________
Example: Virtual → Physical Translation

16-entry Page Table

<table>
<thead>
<tr>
<th>0</th>
<th>0</th>
<th>0</th>
<th>1</th>
<th>2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>--</td>
<td>--</td>
<td>0</td>
<td>--</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>4</td>
</tr>
<tr>
<td>3</td>
<td>--</td>
<td>--</td>
<td>0</td>
<td>--</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>6</td>
<td>--</td>
<td>--</td>
<td>0</td>
<td>--</td>
</tr>
<tr>
<td>7</td>
<td>--</td>
<td>--</td>
<td>0</td>
<td>--</td>
</tr>
<tr>
<td>8</td>
<td>--</td>
<td>--</td>
<td>0</td>
<td>--</td>
</tr>
<tr>
<td>9</td>
<td>--</td>
<td>--</td>
<td>0</td>
<td>--</td>
</tr>
<tr>
<td>A</td>
<td>--</td>
<td>--</td>
<td>0</td>
<td>--</td>
</tr>
<tr>
<td>B</td>
<td>--</td>
<td>--</td>
<td>0</td>
<td>--</td>
</tr>
<tr>
<td>C</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>7</td>
</tr>
<tr>
<td>D</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>6</td>
</tr>
<tr>
<td>E</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>5</td>
</tr>
<tr>
<td>F</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>3</td>
</tr>
</tbody>
</table>


| VPN 0x4 | 0x000 | 0x0FC |
| VPN 0x5 | 0x100 | 0x1FC |
| VPN 0x0 | 0x200 | 0x2FC |
| VPN 0xF | 0x300 | 0x3FC |
| VPN 0x2 | 0x400 | 0x4FC |
| VPN 0xE | 0x500 | 0x5FC |
| VPN 0xD | 0x600 | 0x6FC |
| VPN 0xC | 0x700 | 0x7FC |

Setup:
- 256 bytes/page ($2^8$)
- 16 virtual pages ($2^4$)
- 8 physical pages ($2^3$)
- 12-bit VA (4 vpn, 8 offset)
- 11-bit PA (3 ppn, 8 offset)

$\text{lwm } 0x2C8(x0)$

VA = 0x2C8, PA = ________
Example: Virtual $\rightarrow$ Physical Translation

**16-entry Page Table**

<table>
<thead>
<tr>
<th>0</th>
<th>0</th>
<th>0</th>
<th>1</th>
<th>2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>--</td>
<td>--</td>
<td>0</td>
<td>--</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>4</td>
</tr>
<tr>
<td>3</td>
<td>--</td>
<td>--</td>
<td>0</td>
<td>--</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>6</td>
<td>--</td>
<td>--</td>
<td>0</td>
<td>--</td>
</tr>
<tr>
<td>7</td>
<td>--</td>
<td>--</td>
<td>0</td>
<td>--</td>
</tr>
<tr>
<td>8</td>
<td>--</td>
<td>--</td>
<td>0</td>
<td>--</td>
</tr>
<tr>
<td>9</td>
<td>--</td>
<td>--</td>
<td>0</td>
<td>--</td>
</tr>
<tr>
<td>A</td>
<td>--</td>
<td>--</td>
<td>0</td>
<td>--</td>
</tr>
<tr>
<td>B</td>
<td>--</td>
<td>--</td>
<td>0</td>
<td>--</td>
</tr>
<tr>
<td>C</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>7</td>
</tr>
<tr>
<td>D</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>6</td>
</tr>
<tr>
<td>E</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>5</td>
</tr>
<tr>
<td>F</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>3</td>
</tr>
</tbody>
</table>

**8-page Phys. Mem.**

- VPN 0x4: VA = 0x000, PA = 0x0FC
- VPN 0x5: VA = 0x100, PA = 0x1FC
- VPN 0x0: VA = 0x200, PA = 0x2FC
- VPN 0xF: VA = 0x300, PA = 0x3FC
- VPN 0x2: VA = 0x400, PA = 0x4FC
- VPN 0xE: VA = 0x500, PA = 0x5FC
- VPN 0xD: VA = 0x600, PA = 0x6FC
- VPN 0xC: VA = 0x700, PA = 0x7FC

**Setup:**
- 256 bytes/page ($2^8$)
- 16 virtual pages ($2^4$)
- 8 physical pages ($2^3$)
- 12-bit VA (4 vpn, 8 offset)
- 11-bit PA (3 pnn, 8 offset)

**Example:**

- lw 0x2C8(x0)
  - VA = 0x2C8
  - VPN = 0x2
Example: Virtual → Physical Translation

16-entry Page Table


Setup:
256 bytes/page \(2^8\)
16 virtual pages \(2^4\)
8 physical pages \(2^3\)
12-bit VA (4 vpn, 8 offset)
11-bit PA (3 ppp, 8 offset)

lw 0x2C8(x0)
VA = 0x2C8, PA = _______
VPN = 0x2
### Example: Virtual → Physical Translation

#### 16-entry Page Table

<table>
<thead>
<tr>
<th>D</th>
<th>W</th>
<th>R</th>
<th>PPN</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>1</td>
<td>--</td>
<td>--</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>--</td>
<td>--</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>6</td>
<td>--</td>
<td>--</td>
<td>0</td>
</tr>
<tr>
<td>7</td>
<td>--</td>
<td>--</td>
<td>0</td>
</tr>
<tr>
<td>8</td>
<td>--</td>
<td>--</td>
<td>0</td>
</tr>
<tr>
<td>9</td>
<td>--</td>
<td>--</td>
<td>0</td>
</tr>
<tr>
<td>A</td>
<td>--</td>
<td>--</td>
<td>0</td>
</tr>
<tr>
<td>B</td>
<td>--</td>
<td>--</td>
<td>0</td>
</tr>
<tr>
<td>C</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>D</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>E</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>F</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>


- VPN 0x4
  - VA = 0x200
  - PPN = 0x4
- VPN 0x5
- VPN 0x0
- VPN 0xF
- VPN 0x2
- VPN 0xE
- VPN 0xC

#### Setup:
- 256 bytes/page \((2^8)\)
- 16 virtual pages \((2^4)\)
- 8 physical pages \((2^3)\)
- 12-bit VA (4 vpn, 8 offset)
- 11-bit PA (3 ppn, 8 offset)

- \(\text{lw } 0x2C8(x0)\)
  - VA = 0x2C8
  - PPN = 0x4

- VPN = 0x2
  - → PPN = 0x4
Example: Virtual \(\rightarrow\) Physical Translation

**16-entry Page Table**

<table>
<thead>
<tr>
<th>D</th>
<th>W</th>
<th>R</th>
<th>PPN</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>1</td>
<td>--</td>
<td>--</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>--</td>
<td>--</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>6</td>
<td>--</td>
<td>--</td>
<td>0</td>
</tr>
<tr>
<td>7</td>
<td>--</td>
<td>--</td>
<td>0</td>
</tr>
<tr>
<td>8</td>
<td>--</td>
<td>--</td>
<td>0</td>
</tr>
<tr>
<td>9</td>
<td>--</td>
<td>--</td>
<td>0</td>
</tr>
<tr>
<td>A</td>
<td>--</td>
<td>--</td>
<td>0</td>
</tr>
<tr>
<td>B</td>
<td>--</td>
<td>--</td>
<td>0</td>
</tr>
<tr>
<td>C</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>D</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>E</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>F</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

**8-page Phys. Mem.**

- **VPN 0x4**
  - VA: 0x000
  - PA: ___________ 0x0FC
- **VPN 0x5**
  - VA: 0x100
  - PA: ___________ 0x1FC
- **VPN 0x0**
  - VA: 0x200
  - PA: ___________ 0x2FC
- **VPN 0xF**
  - VA: 0x300
  - PA: ___________ 0x3FC
- **VPN 0x2**
  - VA: 0x400
  - PA: ___________ 0x4FC
- **VPN 0xE**
  - VA: 0x500
  - PA: ___________ 0x5FC
- **VPN 0xD**
  - VA: 0x600
  - PA: ___________ 0x6FC
- **VPN 0xC**
  - VA: 0x700
  - PA: ___________ 0x7FC

**Setup:**
- 256 bytes/page \(2^8\)
- 16 virtual pages \(2^4\)
- 8 physical pages \(2^3\)
- 12-bit VA (4 vpn, 8 offset)
- 11-bit PA (3 ppn, 8 offset)

**lw 0x2C8(x0)**

VA = 0x2C8, PA = \[0x4C8\]

VPN = 0x2

→ PPN = 0x4
Caching vs. Demand Paging

**Caching**
- cache entry
- cache block (~32 bytes)
- cache miss rate (1% to 20%)
- cache hit (~1 cycle)
- cache miss (~100 cycles)
- a miss is handled in *hardware*

**Demand paging**
- page frame
- page (~4K bytes)
- page miss rate (<0.001%)
- page hit (~100 cycles)
- page miss (~5M cycles)
- a miss is handled mostly in *software*
An access to a page that does not have a valid translation causes a page fault exception. OS page fault handler is invoked, handles miss:

- Choose a page to replace, write it back if dirty. Mark page as no longer resident.
Page Faults

An access to a page that does not have a valid translation causes a page fault exception. OS page fault handler is invoked, handles miss:

- Choose a page to replace, write it back if dirty. Mark page as no longer resident
- Read page from disk into available physical page
Page Faults

An access to a page that does not have a valid translation causes a page fault exception. OS page fault handler is invoked, handles miss:

- Choose a page to replace, write it back if dirty. Mark page as no longer resident
- Read page from disk into available physical page
- Update page table to show new page is resident
Page Faults

An access to a page that does not have a valid translation causes a page fault exception. OS page fault handler is invoked, handles miss:

- Choose a page to replace, write it back if dirty. Mark page as no longer resident
- Read page from disk into available physical page
- Update page table to show new page is resident
- Return control to program, which re-executes memory access

![Diagram showing page fault before and after](chart.png)
Translation Lookaside Buffer (TLB)

Problem: Address translation is very expensive! Each reference requires accessing page table

Solution: *Cache translations in TLB*

- TLB hit $\Rightarrow$ *Single-cycle Translation*
- TLB miss $\Rightarrow$ *Page Table Walk to refill*

---

<table>
<thead>
<tr>
<th>V</th>
<th>R</th>
<th>W</th>
<th>D</th>
<th>tag</th>
<th>PPN</th>
</tr>
</thead>
</table>

*(VPN = virtual page number)*

*(PPN = physical page number)*

---

virtual address

physical address

VPN offset

fault? hit?
TLB Designs

• Typically 32-128 entries, 4 to 8-way set-associative
TLB Designs

- Typically 32-128 entries, 4 to 8-way set-associative
  - Modern processors use a hierarchy of TLBs
    (e.g., 128-entry L1 TLB + 2K-entry L2 TLB)
TLB Designs

- Typically 32-128 entries, 4 to 8-way set-associative
  - Modern processors use a hierarchy of TLBs (e.g., 128-entry L1 TLB + 2K-entry L2 TLB)

- Switching processes is expensive because TLB has to be flushed
TLB Designs

• Typically 32-128 entries, 4 to 8-way set-associative
  – Modern processors use a hierarchy of TLBs
    (e.g., 128-entry L1 TLB + 2K-entry L2 TLB)

• Switching processes is expensive because TLB has to be flushed
  – Alternatively, include process ID in TLB entries to avoid flushing
TLB Designs

• Typically 32-128 entries, 4 to 8-way set-associative
  – Modern processors use a hierarchy of TLBs (e.g., 128-entry L1 TLB + 2K-entry L2 TLB)

• Switching processes is expensive because TLB has to be flushed
  – Alternatively, include process ID in TLB entries to avoid flushing

• Handling a TLB miss: “Walk” the page table; if the page is in memory, load the VPN→PPN translation in the TLB. Otherwise, cause a page fault
TLB Designs

- Typically 32-128 entries, 4 to 8-way set-associative
  - Modern processors use a hierarchy of TLBs (e.g., 128-entry L1 TLB + 2K-entry L2 TLB)

- Switching processes is expensive because TLB has to be flushed
  - Alternatively, include process ID in TLB entries to avoid flushing

- Handling a TLB miss: “Walk” the page table; if the page is in memory, load the VPN → PPN translation in the TLB. Otherwise, cause a page fault
  - Page faults are always handled in software
TLB Designs

- Typically 32-128 entries, 4 to 8-way set-associative
  - Modern processors use a hierarchy of TLBs (e.g., 128-entry L1 TLB + 2K-entry L2 TLB)

- Switching processes is expensive because TLB has to be flushed
  - Alternatively, include process ID in TLB entries to avoid flushing

- Handling a TLB miss: “Walk” the page table; if the page is in memory, load the VPN→PPN translation in the TLB. Otherwise, cause a page fault
  - Page faults are always handled in software
  - But page walks are usually handled in hardware using a memory management unit (MMU)
**TLB Designs**

- Typically 32-128 entries, 4 to 8-way set-associative
  - Modern processors use a hierarchy of TLBs (e.g., 128-entry L1 TLB + 2K-entry L2 TLB)

- Switching processes is expensive because TLB has to be flushed
  - Alternatively, include process ID in TLB entries to avoid flushing

- Handling a TLB miss: “Walk” the page table; if the page is in memory, load the VPN → PPN translation in the TLB. Otherwise, cause a page fault
  - Page faults are always handled in software
  - But page walks are usually handled in hardware using a *memory management unit (MMU)*
    - RISC-V, x86 access page table in hardware
Address Translation: *putting it all together*

- **Virtual Address**
- **TLB Lookup**
  - hit
  - **Protection Check**
    - permitted
    - **Physical Address (to mem)**
  - denied
    - **Protection Fault**
  - miss
    - **Page Table Walk**
      - the page is
        - **Page Fault** (OS loads page)
        - **Update TLB**
      - ** logged as SEGFAULT**

Where?

**hardware**
- hardware or software
- software
Example: TLB and Page Table

Suppose

• Virtual memory of $2^{32}$ bytes
• Physical memory of $2^{24}$ bytes
• Page size is $2^{10}$ (1 K) bytes
• 4-entry fully associative TLB

1. How many pages can be stored in physical memory at once?
2. How many entries are there in the page table?
3. How many bits per entry in the page table? (Assume each entry has PPN, resident bit, dirty bit)
4. How many pages does page table take?
5. What fraction of virtual memory can be resident?
6. What is the physical address for virtual address 0x1804? What components are involved in the translation?
7. Same for 0x1080
8. Same for 0x0FC
Example: TLB and Page Table

Suppose

- Virtual memory of $2^{32}$ bytes
- Physical memory of $2^{24}$ bytes
- Page size is $2^{10}$ (1 K) bytes
- 4-entry fully associative TLB

1. How many pages can be stored in physical memory at once? $2^{14}$
2. How many entries are there in the page table?
3. How many bits per entry in the page table? (Assume each entry has PPN, resident bit, dirty bit)
4. How many pages does page table take?
5. What fraction of virtual memory can be resident?
6. What is the physical address for virtual address 0x1804? What components are involved in the translation?
7. Same for 0x1080
8. Same for 0x0FC
Example: TLB and Page Table

Suppose
- Virtual memory of $2^{32}$ bytes
- Physical memory of $2^{24}$ bytes
- Page size is $2^{10}$ (1 K) bytes
- 4-entry fully associative TLB

1. How many pages can be stored in physical memory at once? $2^{14}$
2. How many entries are there in the page table? $2^{22}$
3. How many bits per entry in the page table? (Assume each entry has PPN, resident bit, dirty bit)
4. How many pages does page table take?
5. What fraction of virtual memory can be resident?
6. What is the physical address for virtual address 0x1804? What components are involved in the translation?
7. Same for 0x1080
8. Same for 0x0FC

Page Table

<table>
<thead>
<tr>
<th>VPN</th>
<th>R D PPN</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0 0 7</td>
</tr>
<tr>
<td>1</td>
<td>1 1 9</td>
</tr>
<tr>
<td>2</td>
<td>1 0 0</td>
</tr>
<tr>
<td>3</td>
<td>0 0 5</td>
</tr>
<tr>
<td>4</td>
<td>1 0 5</td>
</tr>
<tr>
<td>5</td>
<td>0 0 3</td>
</tr>
<tr>
<td>6</td>
<td>1 1 2</td>
</tr>
<tr>
<td>7</td>
<td>1 0 4</td>
</tr>
<tr>
<td>8</td>
<td>1 0 1</td>
</tr>
</tbody>
</table>

TLB

Tag Data

<table>
<thead>
<tr>
<th>VPN</th>
<th>R D PPN</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0 0 3</td>
</tr>
<tr>
<td>6</td>
<td>1 1 2</td>
</tr>
<tr>
<td>1</td>
<td>1 1 9</td>
</tr>
<tr>
<td>3</td>
<td>0 0 5</td>
</tr>
<tr>
<td>4</td>
<td>1 0 5</td>
</tr>
<tr>
<td>5</td>
<td>0 0 3</td>
</tr>
<tr>
<td>6</td>
<td>1 1 2</td>
</tr>
<tr>
<td>7</td>
<td>1 0 4</td>
</tr>
<tr>
<td>8</td>
<td>1 0 1</td>
</tr>
</tbody>
</table>

VPN R D PPN
Example: TLB and Page Table

Suppose
- Virtual memory of $2^{32}$ bytes
- Physical memory of $2^{24}$ bytes
- Page size is $2^{10}$ (1 K) bytes
- 4-entry fully associative TLB

<table>
<thead>
<tr>
<th>VPN</th>
<th>R</th>
<th>D</th>
<th>PPN</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>1</td>
<td>9</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
<td>7</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>1</td>
<td>9</td>
</tr>
<tr>
<td>6</td>
<td>1</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>7</td>
<td>0</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>8</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

1. How many pages can be stored in physical memory at once? $2^{14}$
2. How many entries are there in the page table? $2^{22}$
3. How many bits per entry in the page table? (Assume each entry has PPN, resident bit, dirty bit) 16
4. How many pages does page table take?
5. What fraction of virtual memory can be resident?
6. What is the physical address for virtual address 0x1804? What components are involved in the translation?
7. Same for 0x1080
8. Same for 0x0FC
Example: TLB and Page Table

Suppose
- Virtual memory of $2^{32}$ bytes
- Physical memory of $2^{24}$ bytes
- Page size is $2^{10}$ (1 K) bytes
- 4-entry fully associative TLB

<table>
<thead>
<tr>
<th>VPN</th>
<th>R</th>
<th>D</th>
<th>PPN</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>7</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>9</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>5</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>6</td>
<td>1</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>7</td>
<td>1</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td>8</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>...</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1. How many pages can be stored in physical memory at once? $2^{14}$
2. How many entries are there in the page table? $2^{22}$
3. How many bits per entry in the page table? (Assume each entry has PPN, resident bit, dirty bit) 16
4. How many pages does page table take? $2^{23}$ bytes = $2^{13}$ pages
5. What fraction of virtual memory can be resident?
6. What is the physical address for virtual address 0x1804? What components are involved in the translation?
7. Same for 0x1080
8. Same for 0x0FC

April 12, 2018
Example: TLB and Page Table

Suppose
- Virtual memory of $2^{32}$ bytes
- Physical memory of $2^{24}$ bytes
- Page size is $2^{10}$ (1 K) bytes
- 4-entry fully associative TLB

1. How many pages can be stored in physical memory at once? $2^{14}$
2. How many entries are there in the page table? $2^{22}$
3. How many bits per entry in the page table? (Assume each entry has PPN, resident bit, dirty bit) 16
4. How many pages does page table take? $2^{23}$ bytes = $2^{13}$ pages
5. What fraction of virtual memory can be resident? $1/2^8$
6. What is the physical address for virtual address 0x1804? What components are involved in the translation?
7. Same for 0x1080
8. Same for 0x0FC
Example: TLB and Page Table

Suppose
- Virtual memory of $2^{32}$ bytes
- Physical memory of $2^{24}$ bytes
- Page size is $2^{10}$ (1 K) bytes
- 4-entry fully associative TLB

1. How many pages can be stored in physical memory at once? $2^{14}$
2. How many entries are there in the page table? $2^{22}$
3. How many bits per entry in the page table? (Assume each entry has PPN, resident bit, dirty bit) 16
4. How many pages does page table take? $2^{23}$ bytes = $2^{13}$ pages
5. What fraction of virtual memory can be resident? $1/2^8$
6. What is the physical address for virtual address 0x1804? What components are involved in the translation? [VPN=6] 0x804
7. Same for 0x1080
8. Same for 0x0FC
Example: TLB and Page Table

Suppose

- Virtual memory of $2^{32}$ bytes
- Physical memory of $2^{24}$ bytes
- Page size is $2^{10}$ (1 K) bytes
- 4-entry fully associative TLB

1. How many pages can be stored in physical memory at once? $2^{14}$
2. How many entries are there in the page table? $2^{22}$
3. How many bits per entry in the page table? (Assume each entry has PPN, resident bit, dirty bit) 16
4. How many pages does page table take? $2^{23}$ bytes = $2^{13}$ pages
5. What fraction of virtual memory can be resident? $1/2^8$
6. What is the physical address for virtual address 0x1804? What components are involved in the translation? [VPN=6] 0x804
7. Same for 0x1080 [VPN=4] 0x1480
8. Same for 0x0FC
Example: TLB and Page Table

Suppose
- Virtual memory of $2^{32}$ bytes
- Physical memory of $2^{24}$ bytes
- Page size is $2^{10}$ (1 K) bytes
- 4-entry fully associative TLB

1. How many pages can be stored in physical memory at once? $2^{14}$
2. How many entries are there in the page table? $2^{22}$
3. How many bits per entry in the page table? (Assume each entry has PPN, resident bit, dirty bit) 16
4. How many pages does page table take? $2^{23}$ bytes $= 2^{13}$ pages
5. What fraction of virtual memory can be resident? $1/2^8$
6. What is the physical address for virtual address 0x1804? What components are involved in the translation? [VPN=6] 0x804
7. Same for 0x1080 [VPN=4] 0x1480
8. Same for 0x0FC [VPN=0] page fault
Problem: Size of Linear Page Table

With 32-bit addresses, 4 KB pages & 4-byte PTEs:

⇒ $2^{20}$ PTEs, i.e, 4 MB page table per process
⇒ We often have hundreds to thousands of processes per machine... use GBs of memory just for page tables?
Problem: Size of Linear Page Table

With 32-bit addresses, 4 KB pages & 4-byte PTEs:
  ⇒ $2^{20}$ PTEs, i.e, 4 MB page table per process
  ⇒ We often have hundreds to thousands of processes per machine... use GBs of memory just for page tables?

Use larger pages?
  • Internal fragmentation (not all memory in a page is used)
  • Larger page fault penalty (more time to read from disk)
Problem: Size of Linear Page Table

With 32-bit addresses, 4 KB pages & 4-byte PTEs:

⇒ \(2^{20}\) PTEs, i.e., 4 MB page table per process
⇒ We often have hundreds to thousands of processes per machine... use GBs of memory just for page tables?

Use larger pages?

- Internal fragmentation (not all memory in a page is used)
- Larger page fault penalty (more time to read from disk)

What about a 64-bit virtual address space?

- Even 1MB pages would require \(2^{44}\) 8-byte PTEs (35 TB!)
Problem: Size of Linear Page Table

With 32-bit addresses, 4 KB pages & 4-byte PTEs:

⇒ $2^{20}$ PTEs, i.e, 4 MB page table *per process*
⇒ We often have hundreds to thousands of processes per machine... use GBs of memory just for page tables?

Use larger pages?

• Internal fragmentation (not all memory in a page is used)
• Larger page fault penalty (more time to read from disk)

What about a 64-bit virtual address space?

• Even 1MB pages would require $2^{44}$ 8-byte PTEs (35 TB!)

Solution: Use a sparse page table format (size proportional to amount of *mapped* pages)
Hierarchical Page Table

Virtual Address

31  22  21  12  11  0

p1  p2  offset

10-bit  10-bit
L1 index  L2 index

Root of the Current Page Table

(Processor Register)

Level 1 Page Table

p1

Level 2 Page Tables

offset

Data Pages

page in primary memory
page in secondary memory
PTE of a nonexistent page
Using Caches with Virtual Memory

**Virtually-Addressed Cache**

- FAST: No virtual → physical translation on HIT
- Problem: Must flush cache after context switch
Using Caches with Virtual Memory

**Virtually-Addressed Cache**
- FAST: No virtual→physical translation on HIT
- Problem: Must flush cache after context switch

**Physically-Addressed Cache**
- Avoids stale cache data after context switch
- SLOW: Virtual→physical time on HIT
OBSERVATION: If cache index bits are a subset of page offset bits, tag access in a physical cache can *overlap* TLB access. Tag from cache is compared with physical page address from TLB to determine hit/miss.
Best of Both Worlds: Virtually-Indexed, Physically-Tagged Cache (VIPT)

OBSERVATION: If cache index bits are a subset of page offset bits, tag access in a physical cache can overlap TLB access. Tag from cache is compared with physical page address from TLB to determine hit/miss.

Cache index comes entirely from address bits in page offset – don’t need to wait for TLB to start cache lookup!
Best of Both Worlds: Virtually-Indexed, Physically-Tagged Cache (VIPT)

OBSERVATION: If cache index bits are a subset of page offset bits, tag access in a physical cache can overlap TLB access. Tag from cache is compared with physical page address from TLB to determine hit/miss.

Problem: Limits # of bits of cache index → can only increase cache capacity by increasing associativity!
Thank you!

Next lecture: Pipelining