Problem 1.

Consider the following sequential logic circuit. It consists of one input IN, a 2-bit register that stores the current state, and some combinational logic that determines the state (next value to load into the register) based on the current state and the input IN.

(A) Using the timing specifications shown below for the XOR and DREG components, determine the shortest clock period, t\text{CLK}, that will allow the circuit to operate correctly or write NONE if no choice for t\text{CLK} will allow the circuit to operate correctly and briefly explain why.

<table>
<thead>
<tr>
<th>Component</th>
<th>t_{CD}</th>
<th>t_{PD}</th>
<th>t_{SETUP}</th>
<th>t_{HOLD}</th>
</tr>
</thead>
<tbody>
<tr>
<td>XOR2</td>
<td>0.15ns</td>
<td>2.1ns</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>DREG</td>
<td>0.1ns</td>
<td>1.6ns</td>
<td>0.4ns</td>
<td>0.2ns</td>
</tr>
</tbody>
</table>

Minimum value for t\text{CLK (ns)}: _______ or explain why none exists

(B) One of the engineers on the team suggests using a new, faster XOR2 gate with t_{CD} = 0.05ns and t_{PD} = 0.7ns. Determine a new minimum value for t_{CLK} or write NONE and explain why no such value exists.

Minimum value for t\text{CLK (ns)}: _______ or explain why none exists
Problem 2.

Consider the following sequential logic circuit. It consists of three D registers, three different pieces of combinational logic (CL1, CL2, and CL3), one input IN, and one output OUT. The propagation delay, contamination delay, and setup time of the registers are all the same and are specified below each register. The hold time for the registers is **NOT the same** and is specified in bold below each register. The timing specification for each combinational logic block is shown below that logic.

![Diagram of sequential logic circuit]

(A) What is the smallest value for the \( t_{CD} \) of CL2 that will allow all the registers in the circuit to operate correctly?

Smallest value for \( t_{CD} \) of CL2 (ns): __________

(B) What is the smallest value for the period of CLK (i.e., \( t_{CLK} \)) that will allow all the registers in the circuit to operate correctly?

Smallest value for \( t_{CLK} \) (ns): __________

(C) What are the propagation delay and contamination delay of the output, OUT, of this circuit relative to the rising edge of the clock?

\( t_{PD} \) for OUT (ns): __________

\( t_{CD} \) for OUT (ns): __________
Problem 3.

Consider the following sequential logic circuit. The timing specifications are shown below each component. Note that the two registers do NOT have the same specifications.

(A) What is the smallest value for the period of CLK (i.e., tCLK) that will allow both registers in the circuit to operate correctly?

Smallest value for tCLK (ns): __________

(B) What is the smallest value for the tCD of R1 that will allow both registers in the circuit to operate correctly?

Smallest value for tCD of R1 (ns): __________

(C) Suppose two of these sequential circuits were connected in series, with the OUT signal of the first circuit connected to the IN signal of the second circuit. The same CLK signal is used for both circuits. Now what is the smallest value for the period of CLK (i.e., tCLK) that will allow both registers in the circuit to operate correctly?

Smallest value for tCLK (ns): __________
Problem 4.

Consider a "divisible-by-3" FSM that accepts a binary number entered one bit at a time, most significant bit first. The FSM has a one-bit output that indicates if the number entered so far is divisible by 3.

If the value of the number entered so far is $N$, then after the digit $b$ is entered, the value of the new number $N'$ is $2N + b$. This leads to the following transition diagram where the states are labeled with the value of $N \mod 3$.

(A) Construct a truth table for the FSM logic. Inputs include the state bits and the next bit of the number; outputs include the next state bits and the output.

(B) Based on the truth table, implement the FSM using D flip-flops.
**Problem 5.**

In this problem, we construct a sequential circuit to compute the \( N^{\text{th}} \) Fibonacci number denoted by \( F_N \). The following recurrence relation defines the Fibonacci sequence.

\[
F_0 = 0, \ F_1 = 1, \ F_N = F_{N-1} + F_{N-2} \quad \forall \ N \geq 2
\]

The circuit is similar to the GCD circuit discussed in the lecture. There are two registers \( x \) and \( y \) that store the Fibonacci values for two consecutive integers. In addition, a counter register \( i \) is initialized to \( N-1 \) and decremented each cycle. The computation stops when register \( i \) goes down to 0 and the result \( (F_N) \) is available in register \( x \).

(A) What are the initial values for registers \( x \) and \( y \)?

(B) Derive the next state computation equations for the three registers.

(C) Derive the logic for the enable signal that determines when the registers are updated using the next state logic. Note that all three registers are controlled by a single enable signal.

(D) Implement the sequential circuit using the next state and enable logic derived above.