6.004 Fall 2018
L13 – The Memory Hierarchy
Take-Home Problem

Due at the beginning of recitation R13 on Wednesday October 24.

A) Given a cache with the following parameters, specify which bits of a 32 bit memory address are used for the block offset, which bits for the index (or set selection) and which bits are used for the tag.

Cache size: 256 data words
Block size: 16 words
Associativity: 2-way

Block offset bits: _________
Index bits: _________
Tag bits: _________

B) How many sets are in the cache of problem A?

Number of sets: _________

C) Determine the number of bits in each set of the cache. Make sure to account for a valid bit, a tag, and all of the data words in each way of the set.

Bits per set: _________