Due at the beginning of recitation R14 on Friday October 26.

Describe a situation where a 1-way Direct-mapped Cache would get a miss but a 2-way Set-associative Cache would not.

Ans)

Let’s assume two memory addresses with the same INDEX field (for cache) but not the same tags.

Assuming t0 and t1 hold Addr_a and Addr_b ( Reg[t0] = Addr_a, Reg[t1] = Addr_b )

And Our program’s memory access pattern is:
   lw t3, 0(t0)
   lw t4, 0(t1) // comes after lw t3,0(t0)
   and repeats such memory reads. (Read from Addr_a -> Addr_b -> Addr_a -> Addr_b …)

Direct-mapped Cache:
   Every loads will trigger a Cache miss since the tags of Addr_a and Addr_b are different but have the same index.

Two-way Set-associative Cache:
   Both values Mem[Addr_a] and Mem[Addr_b] will stay in each of the ways, so even if they have a conflict index, both can be stored in the cache (but in a different way) and there is no Cache misses.