Due at the beginning of recitation R15 on Friday October 31.

1) Pipeline the following circuit for maximum throughput while minimizing latency. The number in each module is the module’s latency.

2) What is the latency and throughput of your pipelined circuit?
   \[
   K = 4 \\
   t_{CLK} = 4 \\
   \text{Latency} = K \cdot t_{CLK} = 4 \cdot 4 = 16 \\
   \text{Throughput} = \frac{1}{t_{CLK}} = \frac{1}{4} = 0.25
   \]