Virtual Memory

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Computer Science & Artificial Intelligence Lab
M.I.T.
Reminder: Operating Systems

- Goals of OS:
  - Protection and privacy: Processes cannot access each other’s data
  - Abstraction: Hide away details of underlying hardware
    - e.g., processes open and access files instead of issuing raw commands to hard drive
  - Resource management: Controls how processes share hardware resources (CPU, memory, disk, etc.)
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Key enabling technologies:
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  - User mode + supervisor mode
  - Interrupts to safely transition into supervisor mode
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Today
Virtual Memory (VM) Systems

*Illusion of a large, private, uniform store*

- Protection & Privacy
  - Each process has a private address space
Virtual Memory (VM) Systems

*Illusion of a large, private, uniform store*

- **Protection & Privacy**
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- **Demand Paging**
  - Provides the ability to run programs larger than main memory
  - Hides differences in machine configuration
Virtual Memory (VM) Systems

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  - Provides the ability to run programs larger than main memory
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The price of VM is address translation on each memory reference
Names for Memory Locations

- Machine language address
  - As specified in machine code

- Virtual address
  - ISA specifies translation of machine code address into virtual address of program variable (sometimes called effective address)

- Physical address
  - Operating system specifies mapping of virtual address into name for a physical memory location
Names for Memory Locations

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- Physical address
  - Operating system specifies mapping of virtual address into name for a physical memory location
Segmentation (Base-and-Bound) Address Translation

- Process Address Space
  - 0x0 to 0x0fff

- Physical Memory
  - 0x0 to 0xf..ff
Each program’s data is allocated in a contiguous segment of physical memory.
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Segmentation (Base-and-Bound) Address Translation

- Each program’s data is allocated in a contiguous segment of physical memory
- Physical address = Virtual Address + Segment Base

Address Space

Virtual Address

Physical Address

Base Reg

Physical Memory

Process Code & Data

0x0

0xf..ff

0x0
Each program’s data is allocated in a contiguous segment of physical memory.

Physical address = Virtual Address + Segment Base

Bound register provides safety and isolation.
Segmentation (Base-and-Bound) Address Translation

- Each program’s data is allocated in a contiguous segment of physical memory
- Physical address = Virtual Address + Segment Base
- Bound register provides safety and isolation
- Base and Bound registers should not be accessed by user programs (only accessible in supervisor mode)
Separate Segments for Code and Data

Load X

Program Address Space

Virtual Address

Data Bound Register

Data Base Register

Main Memory

data segment

code segment

Code Bound Register

Program Counter

Code Base Register

Program Counter

Code Bound Register

Main Memory

data segment

code segment

Bounds Violation?

Bounds Violation?

+
Separate Segments for Code and Data

Pros of this separation?
Separate Segments for Code and Data

Pros of this separation?
Prevents buggy program from overwriting code
Separate Segments for Code and Data

Pros of this separation?
Prevents buggy program from overwriting code
Multiple processes can share code segment
Memory Fragmentation

<table>
<thead>
<tr>
<th>OS Space</th>
<th>proc 1</th>
<th>proc 2</th>
<th>proc 3</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>16K</td>
<td>24K</td>
<td>32K</td>
</tr>
<tr>
<td></td>
<td></td>
<td>24K</td>
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</tbody>
</table>
Memory Fragmentation

Processes 4 & 5 start

OS Space

proc 1
16K

proc 2
24K
24K
24K

proc 3
32K
24K

free
## Memory Fragmentation

<table>
<thead>
<tr>
<th>Process</th>
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</tr>
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<tbody>
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Processes 4 & 5 start:

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<tr>
<td>proc 4</td>
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<td>32K</td>
</tr>
<tr>
<td>proc 5</td>
<td>24K</td>
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</tbody>
</table>
Memory Fragmentation

Processes 4 & 5 start

Processes 2 & 5 end

OS Space

proc 1
16K

proc 2
24K

proc 3
24K

proc 4
16K

proc 5
24K

OS Space

proc 1
16K

proc 2
24K

proc 3
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proc 4
8K

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free
Memory Fragmentation

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<td>24K</td>
<td></td>
</tr>
<tr>
<td>proc 5</td>
<td>24K</td>
</tr>
</tbody>
</table>

**Processes 4 & 5 start**

- proc 4 starts
- proc 5 starts

**Processes 2 & 5 end**

- proc 2 ends
- proc 5 ends

**Free space**
As processes start and end, storage is “fragmented”. Therefore, at some point segments have to be moved around to compact the free space.
Paged Memory Systems

- Divide physical memory in fixed-size blocks called pages
  - Typical page size: 4KB
Paged Memory Systems

- Divide physical memory in fixed-size blocks called **pages**
  - Typical page size: 4KB

- Interpret each virtual address as a pair
  <virtual page number, offset>
Paged Memory Systems

- Divide physical memory in fixed-size blocks called **pages**
  - Typical page size: 4KB

- Interpret each virtual address as a pair `<virtual page number, offset>`

- Use a **page table** to translate from virtual to physical page numbers
  - Page table contains the physical page number (i.e., starting physical address) for each virtual page number
Private Address Space per Process

- Each process has a page table
- Page table has an entry for each process page
Private Address Space per Process

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Page tables make it possible to store the pages of a program non-contiguously
Paging vs. Segmentation

Pros of paging vs segmentation?
Pros of paging vs segmentation?

Paging avoids fragmentation issues
Paging vs. Segmentation

Pros of paging vs segmentation?

Paging avoids fragmentation issues

Paging allows programs that use more virtual memory than the machine’s physical memory (demand paging)
Paging vs. Segmentation

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Page tables are MUCH larger than base & bound regs!
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Page tables are MUCH larger than base & bound regs!

...where do we store the page tables?
Suppose Page Tables reside in memory
Suppose Page Tables reside in memory

Virtual Page Number

VPN  offset  PT Base Reg

Kernel PT Base

PT Proc 1

PT Proc 2

Kernel PT

PTB Proc i
Suppose Page Tables reside in memory

Virtual Page Number

VPN  offset

PT Base Reg

Kernel PT Base

Kernel PT

PT Proc 1

PT Proc 2

PTB Proc \( i \)

Physical Page Number

VPN  offset

PT Proc 1

PT Proc 2

PTB Proc \( i \)
Suppose Page Tables reside in memory
Suppose Page Tables reside in memory

Virtual Page Number

VPN

offset

PT Base Reg

Kernel PT Base

Kernel PT

PT Proc 1

PT Proc 2

PTB Proc $i$

Physical Page Number

VPN

offset

PT Base Reg

PT Proc 1

PT Proc 2

Kernel PT

PTB Proc $i$
Suppose Page Tables reside in memory

VPN | offset
---|---
Virtual Page Number

PT Base Reg

Kernel PT Base

PT Proc 1

PT Proc 2

Kernel PT

Physical Page Number

PTB Proc i

Virtual Page Number + offset → PT Base Reg

Physical Page Number
Suppose Page Tables reside in memory

Translation:
- PPN = Mem[PT Base + VPN]
- PA = PPN + offset
Suppose Page Tables reside in memory

- Translation:
  - PPN = Mem[PT Base + VPN]
  - PA = PPN + offset

- All links represent physical addresses; no VA to PA translation
Suppose Page Tables reside in memory

- **Translation:**
  - \( \text{PPN} = \text{Mem}[\text{PT Base} + \text{VPN}] \)
  - \( \text{PA} = \text{PPN} + \text{offset} \)

- All links represent physical addresses; no VA to PA translation

- On process switch
  - \( \text{PT Base Reg} := \text{Kernel PT Base} + \text{new process ID} \)
Suppose Page Tables reside in memory

- Translation:
  - PPN = Mem[PT Base + VPN]
  - PA = PPN + offset
- All links represent physical addresses; no VA to PA translation
- On process switch
  - PT Base Reg := Kernel PT Base + new process ID

Translation:

Accessing one data word or instruction requires two DRAM accesses!
Paging Implementation Issues

- How to reduce memory access overhead
  - A good VM design must be fast and space-efficient

- What if all the pages can’t fit in DRAM?
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{Beyond the scope of 6.004}
Demand Paging

*Using main memory as a cache of disk*

- All the pages of the processes may not fit in main memory. Therefore, DRAM is backed up by *swap space* on disk.
- Page Table Entry (PTE) contains:
Demand Paging

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- Page Table Entry (PTE) contains:
  - VPN
  - Offset
  - PT Base Reg
Demand Paging

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- Even if all pages fit in memory, demand paging allows bringing only what is needed from disk
Demand Paging
Using main memory as a cache of disk

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- Page Table Entry (PTE) contains:
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  - PPN (physical page number) for a memory-resident page
  - DPN (disk page number) for a page on the disk
  - Protection and usage bits

- Even if all pages fit in memory, demand paging allows bringing only what is needed from disk
  - When a process starts, all code and data are on disk; bring pages in as they are accessed
Example: Virtual \( \rightarrow \) Physical Translation

16-entry Page Table


<table>
<thead>
<tr>
<th>VPN</th>
<th>offset</th>
<th>VA</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>8</td>
<td>VA</td>
</tr>
<tr>
<td>3</td>
<td>8</td>
<td>PA</td>
</tr>
</tbody>
</table>

Setup:
- 256 bytes/page \( (2^8) \)
- 16 virtual pages \( (2^4) \)
- 8 physical pages \( (2^3) \)
- 12-bit VA (4 vpn, 8 offset)
- 11-bit PA (3 ppn, 8 offset)

\[
lw \ 0x2C8(x0) \\
VA = 0x2C8, \ PA = _______
\]
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**lw 0x2C8(x0)**
- VA = 0x2C8, PA = ________

**16-entry Page Table**

<table>
<thead>
<tr>
<th>Index</th>
<th>VPN 0x0</th>
<th>VPN 0x1</th>
<th>VPN 0x2</th>
<th>VPN 0x3</th>
<th>VPN 0x4</th>
<th>VPN 0x5</th>
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</tr>
</tbody>
</table>

**8-page Phys. Mem.**

- VPN 0x0
  - PA = 0x000
- VPN 0x1
  - PA = 0x0FC
- VPN 0x2
  - PA = 0x100
- VPN 0x3
  - PA = 0x1FC
- VPN 0x4
  - PA = 0x200
- VPN 0x5
  - PA = 0x2FC
- VPN 0x6
  - PA = 0x300
- VPN 0x7
  - PA = 0x3FC

**VPN offset**

- VA
  - VPN 0x4, offset 8
  - VPN 0x3, offset 8

**PPN**

- Add dirty condition based on implementation.
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lw 0x2C8(x0)
VA = 0x2C8, PA = ________

16-entry Page Table

<table>
<thead>
<tr>
<th></th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
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- VPN 0x0
- VPN 0x1
- VPN 0x2
- VPN 0x3
- VPN 0x4
- VPN 0x5
- VPN 0x6
- VPN 0x7
- VPN 0x8
- VPN 0x9
- VPN 0xA
- VPN 0xB
- VPN 0xC
- VPN 0xD
- VPN 0xE
- VPN 0xF

VPN offset
- VA
- PA
- PPN

Dirty
Writable
Resident
Example: Virtual → Physical Translation

Setup:
- 256 bytes/page ($2^8$)
- 16 virtual pages ($2^4$)
- 8 physical pages ($2^3$)
- 12-bit VA (4 vpn, 8 offset)
- 11-bit PA (3 ppn, 8 offset)

1w 0x2C8(x0)
VA = 0x2C8, PA = _______

VPN = 0x2
Example: Virtual \(\rightarrow\) Physical Translation

Setup:
256 bytes/page \((2^8)\)
16 virtual pages \((2^4)\)
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\(\text{lw} \ 0x2C8(x0)\)
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Example: Virtual → Physical Translation

16-entry Page Table


Setup:
- 256 bytes/page \(2^8\)
- 16 virtual pages \(2^4\)
- 8 physical pages \(2^3\)
- 12-bit VA (4 vpn, 8 offset)
- 11-bit PA (3 ppn, 8 offset)

lw 0x2C8(x0)
VA = 0x2C8, PA = ________

VPN = 0x2
→ PPN = 0x4
Example: Virtual $\rightarrow$ Physical Translation

16-entry Page Table


<table>
<thead>
<tr>
<th>VPN</th>
<th>offset</th>
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</thead>
<tbody>
<tr>
<td>4</td>
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<tr>
<td>3</td>
<td>8</td>
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</tbody>
</table>

VA

PA

Setup:
- 256 bytes/page ($2^8$)
- 16 virtual pages ($2^4$)
- 8 physical pages ($2^3$)
- 12-bit VA (4 vpn, 8 offset)
- 11-bit PA (3 pnn, 8 offset)

lw 0x2C8(x0)

VA = 0x2C8, PA = 0x4C8

VPN = 0x2

$\rightarrow$ PPN = 0x4
Caching vs. Demand Paging

**Caching**
- cache entry
- cache block (~32 bytes)
- cache miss rate (1% to 20%)
- cache hit (~1 cycle)
- cache miss (~100 cycles)
- a miss is handled in *hardware*

**Demand paging**
- page frame
- page (~4K bytes)
- page miss rate (<0.001%)
- page hit (~100 cycles)
- page miss (~5M cycles)
- a miss is handled mostly in *software*
Page Faults

An access to a page that does not have a valid translation causes a page fault exception. OS page fault handler is invoked, handles miss:

- Choose a page to replace, write it back if dirty. Mark page as no longer resident
Page Faults

An access to a page that does not have a valid translation causes a page fault exception. OS page fault handler is invoked, handles miss:

- Choose a page to replace, write it back if dirty. Mark page as no longer resident
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Page Faults

An access to a page that does not have a valid translation causes a **page fault exception**. OS page fault handler is invoked, handles miss:

- Choose a page to replace, write it back if dirty. Mark page as no longer resident
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- Update page table to show new page is resident
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- Choose a page to replace, write it back if dirty. Mark page as no longer resident
- Read page from disk into available physical page
- Update page table to show new page is resident
- Return control to program, which re-executes memory access
Translation Lookaside Buffer (TLB)

Problem: Address translation is very expensive! Each reference requires accessing page table

Solution: *Cache translations in TLB*

- **TLB hit** ⇒ *Single-cycle Translation*
- **TLB miss** ⇒ *Page Table Walk to refill*

---

**Diagram:**

- **Virtual address**
  - **VPN**
  - **offset**

- **Physical address**
  - **PPN**
  - **offset**

<table>
<thead>
<tr>
<th>V</th>
<th>R</th>
<th>W</th>
<th>D</th>
<th>tag</th>
<th>PPN</th>
</tr>
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<tbody>
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</tr>
</tbody>
</table>

(VPN = virtual page number)
(PPN = physical page number)
TLB Designs

- Typically 32-128 entries, 4 to 8-way set-associative
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  - Modern processors use a hierarchy of TLBs (e.g., 128-entry L1 TLB + 2K-entry L2 TLB)
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- Handling a TLB miss: “Walk” the page table. If the page is in memory, load the VPN→PPN translation in the TLB. Otherwise, cause a page fault
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- Handling a TLB miss: “Walk” the page table. If the page is in memory, load the VPN→PPN translation in the TLB. Otherwise, cause a page fault
  - Page faults are always handled in software
  - But page walks are usually handled in hardware using a memory management unit (MMU)
    - RISC-V, x86 access page table in hardware
Address Translation: Putting it all together

Virtual Address

TLB Lookup

hit

Page Table Walk

the page is ∈ memory

Page Fault (OS loads page)

miss

Update TLB

Page Table Walk

the page is ∈ memory

protected

Protection Check

denied

Protection Fault

permitted

physical Address (to mem)

SEGFAULT

Where?
Example: TLB and Page Table

Suppose
- Virtual memory of $2^{32}$ bytes
- Physical memory of $2^{24}$ bytes
- Page size is $2^{10}$ (1 K) bytes
- 4-entry fully associative TLB

1. How many pages can be stored in physical memory at once?
2. How many entries are there in the page table?
3. How many bits per entry in the page table? (Assume each entry has PPN, resident bit, dirty bit)
4. How many pages does page table take?
5. What fraction of virtual memory can be resident?
6. What is the physical address for virtual address 0x1804? What components are involved in the translation?
7. Same for 0x1080
8. Same for 0x0FC

TLB

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Page Table

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VPN | R | D | PPN
----|---|---|-----
0   | 0 | 0 | 3   
6   | 1 | 1 | 9   
1   | 1 | 9 |     
3   | 0 | 5 |     
4   | 0 | 5 |     
5   | 0 | 3 |     
6   | 1 | 2 |     
7   | 1 | 4 |     
8   | 1 | 1 |     
...
Example: TLB and Page Table

Suppose
- Virtual memory of $2^{32}$ bytes
- Physical memory of $2^{24}$ bytes
- Page size is $2^{10}$ (1 K) bytes
- 4-entry fully associative TLB

1. How many pages can be stored in physical memory at once? $2^{14}$
2. How many entries are there in the page table?
3. How many bits per entry in the page table? (Assume each entry has PPN, resident bit, dirty bit)
4. How many pages does page table take?
5. What fraction of virtual memory can be resident?
6. What is the physical address for virtual address 0x1804? What components are involved in the translation?
7. Same for 0x1080
8. Same for 0x0FC
Example: TLB and Page Table

Suppose
- Virtual memory of $2^{32}$ bytes
- Physical memory of $2^{24}$ bytes
- Page size is $2^{10}$ (1 K) bytes
- 4-entry fully associative TLB

1. How many pages can be stored in physical memory at once? $2^{14}$
2. How many entries are there in the page table? $2^{22}$
3. How many bits per entry in the page table? (Assume each entry has PPN, resident bit, dirty bit)
4. How many pages does page table take?
5. What fraction of virtual memory can be resident?
6. What is the physical address for virtual address 0x1804? What components are involved in the translation?
7. Same for 0x1080
8. Same for 0x0FC
Example: TLB and Page Table

Suppose
- Virtual memory of $2^{32}$ bytes
- Physical memory of $2^{24}$ bytes
- Page size is $2^{10}$ (1 K) bytes
- 4-entry fully associative TLB

1. How many pages can be stored in physical memory at once? $2^{14}$
2. How many entries are there in the page table? $2^{22}$
3. How many bits per entry in the page table? (Assume each entry has PPN, resident bit, dirty bit) 16
4. How many pages does page table take?
5. What fraction of virtual memory can be resident?
6. What is the physical address for virtual address 0x1804? What components are involved in the translation?
7. Same for 0x1080
8. Same for 0x0FC
Example: TLB and Page Table

Suppose

• Virtual memory of $2^{32}$ bytes
• Physical memory of $2^{24}$ bytes
• Page size is $2^{10}$ (1 K) bytes
• 4-entry fully associative TLB

1. How many pages can be stored in physical memory at once? $2^{14}$
2. How many entries are there in the page table? $2^{22}$
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7. Same for 0x1080
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Example: TLB and Page Table

Suppose

• Virtual memory of $2^{32}$ bytes
• Physical memory of $2^{24}$ bytes
• Page size is $2^{10}$ (1 K) bytes
• 4-entry fully associative TLB

1. How many pages can be stored in physical memory at once? $2^{14}$
2. How many entries are there in the page table? $2^{22}$
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4. How many pages does page table take? $2^{23}$ bytes = $2^{13}$ pages
5. What fraction of virtual memory can be resident? $1/2^8$
6. What is the physical address for virtual address 0x1804? What components are involved in the translation?
7. Same for 0x1080
8. Same for 0x0FC

Page Table

TLB

VPN | R   | D   | PPN
---+-----+-----+-----
0  | 0    | 0   | 7
1  | 1    | 1   | 9
2  | 1    | 0   | 0
3  | 0    | 0   | 5
4  | 1    | 0   | 5
5  | 0    | 0   | 3
6  | 1    | 1   | 2
7  | 1    | 0   | 4
8  | 1    | 0   | 1

VPN | R   | D   | PPN
---+-----+-----+-----
0  | 0    | 0   | 3
6  | 1    | 1   | 2
1  | 1    | 1   | 9
3  | 0    | 0   | 5
4  | 1    | 0   | 5
5  | 0    | 0   | 3
6  | 1    | 1   | 2
7  | 1    | 0   | 4
8  | 1    | 0   | 1
...
Example: TLB and Page Table

Suppose

- Virtual memory of $2^{32}$ bytes
- Physical memory of $2^{24}$ bytes
- Page size is $2^{10}$ (1 K) bytes
- 4-entry fully associative TLB

1. How many pages can be stored in physical memory at once? $2^{14}$
2. How many entries are there in the page table? $2^{22}$
3. How many bits per entry in the page table? (Assume each entry has PPN, resident bit, dirty bit) 16
4. How many pages does page table take? $2^{23}$ bytes = $2^{13}$ pages
5. What fraction of virtual memory can be resident? $1/2^8$
6. What is the physical address for virtual address 0x1804? What components are involved in the translation? [VPN=6] 0x804
7. Same for 0x1080
8. Same for 0x0FC
Example: TLB and Page Table

Suppose

- Virtual memory of $2^{32}$ bytes
- Physical memory of $2^{24}$ bytes
- Page size is $2^{10}$ (1 K) bytes
- 4-entry fully associative TLB

1. How many pages can be stored in physical memory at once? $2^{14}$
2. How many entries are there in the page table? $2^{22}$
3. How many bits per entry in the page table? (Assume each entry has PPN, resident bit, dirty bit) 16
4. How many pages does page table take? $2^{23}$ bytes = $2^{13}$ pages
5. What fraction of virtual memory can be resident? $1/2^8$
6. What is the physical address for virtual address 0x1804? What components are involved in the translation? [VPN=6] 0x804
7. Same for 0x1080 [VPN=4] 0x1480
8. Same for 0x0FC

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Page Table

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</table>

November 15, 2018
Example: TLB and Page Table

Suppose
- Virtual memory of $2^{32}$ bytes
- Physical memory of $2^{24}$ bytes
- Page size is $2^{10}$ (1 K) bytes
- 4-entry fully associative TLB

1. How many pages can be stored in physical memory at once? $2^{14}$
2. How many entries are there in the page table? $2^{22}$
3. How many bits per entry in the page table? (Assume each entry has PPN, resident bit, dirty bit) 16
4. How many pages does page table take? $2^{23}$ bytes = $2^{13}$ pages
5. What fraction of virtual memory can be resident? $1/2^8$
6. What is the physical address for virtual address 0x1804? What components are involved in the translation? [VPN=6] 0x804
7. Same for 0x1080 [VPN=4] 0x1480
8. Same for 0x0FC [VPN=0] page fault
Problem: Size of Linear Page Table

With 32-bit addresses, 4 KB pages & 4-byte PTEs:

⇒ $2^{20}$ PTEs, i.e, 4 MB page table per process
⇒ We often have hundreds to thousands of processes per machine... use GBs of memory just for page tables?
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Solution: Use a sparse page table format (size proportional to amount of mapped pages)
Hierarchical Page Table

Virtual Address

31  22  21  12  11  0

p1  p2  offset

10-bit 10-bit
L1 index L2 index

Root of the Current Page Table

(Processor Register)

Level 1 Page Table

Level 2 Page Tables

Data Pages

page in primary memory

page in secondary memory

PTE of a nonexistent page
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- Making paging efficient
  - TLB: Cache the page table
  - Hierarchical page tables: Keep page table size small
Thank you!

Next lecture: I/O and implementation issues of Virtual Memory and Exceptions