Problem 1. Binary Arithmetic (10 points)

(A) (4 points) What is 0x79 << ~(0xFC) where ~ is bitwise NOT and << is bitwise LEFT SHIFT on 8-bit operands? Provide your result in both 8-bit binary and in hexadecimal.

Result in binary (0b):_________________________

Result in hexadecimal (0x):_________________________

(B) (4 points) What is 0b1011 multiplied by 0b0101? You can treat both numbers as unsigned, and the result will be more than four bits. Show how you computed this with binary multiplication. What is this number in decimal?

0b1011 multiplied by 0b0101 (show your work) (0b):_________________________

(in decimal): ___________________

(C) (2 points) What is 0b10110101 in decimal assuming unsigned encoding (only positive integers)? What is it in decimal assuming two’s complement encoding?

0b10110101 assuming unsigned encoding (in decimal):_______________

0b10110101 assuming two’s complement encoding (in decimal):_____________
Problem 2. Boolean Logic (12 points)

(A) (6 points) Simplify the following Boolean expressions by finding a minimal sum-of-products (minimal SOP) expression for each one. (Note: These expressions can be reduced into a minimal SOP by repeatedly applying the Boolean algebra properties we saw in lecture.)

1. \((r + a) \cdot y \cdot ((r + \bar{a}) \cdot \bar{y})\)

2. \((x + y) \cdot z + \bar{z} \cdot x + y \cdot (\bar{x} + z)\)

(B) (6 points) Consider the truth table on the right, which defines function \(Y\) out of three input variables \((A, B,\) and \(C)\).

1. Find a minimal sum-of-products expression for \(Y\).

\[
\begin{array}{ccc|c}
A & B & C & Y \\
0 & 0 & 0 & 0 \\
0 & 0 & 1 & 1 \\
0 & 1 & 0 & 0 \\
0 & 1 & 1 & 0 \\
1 & 0 & 0 & 1 \\
1 & 0 & 1 & 1 \\
1 & 1 & 0 & 0 \\
1 & 1 & 1 & 0 \\
\end{array}
\]

Minimal sum-of-products for \(Y(A,B,C) = \) ________________

2. Using only combinational circuits built from gates specified by the truth table above, which of the following statements are true?

(A) We can implement any Boolean function using only these gates.
(B) We can’t implement every Boolean function using only these gates.
(C) We can only implement functions with the same truth table as above.

Circle all true answers: A … B … C
Problem 3. The Digital Abstraction (14 points)

Rummaging through a box of old circuit components, you find a Q-device with the voltage transfer characteristic (VTC) shown to the right.

(A) (4 points) We want to use the Q-device as a binary digital inverter. Find a set of signaling thresholds \( (V_{OL} < V_{IL} \leq V_{IH} < V_{OH}) \) that maximizes noise immunity (the smallest of the noise margins).

\[
V_{OL} = \_\_\_\_\_\_ V_{IL} = \_\_\_\_\_\_ V_{IH} = \_\_\_\_\_\_ V_{OH} = \_\_\_\_\_\_ \\
\text{Noise Immunity} = \_\_\_\_\_\_
\]

(B) (4 points) Find a different set of signaling thresholds from the one above that also maximizes noise immunity.

\[
V_{OL} = \_\_\_\_\_\_ V_{IL} = \_\_\_\_\_\_ V_{IH} = \_\_\_\_\_\_ V_{OH} = \_\_\_\_\_\_ \\
\text{Noise Immunity} = \_\_\_\_\_\_
\]

Reading the Q-device’s datasheet, you discover that it was meant to be used as a quaternary digital device. In quaternary logic, each voltage represents one of four possible symbols, 0, 1, 2, or 3. (By contrast, in binary logic each voltage represents one of two possible symbols, 0 or 1.)

The Q-device uses the following mapping of quaternary digital symbols to output voltages:

<table>
<thead>
<tr>
<th>Quaternary Symbol</th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{out} )</td>
<td>0 V</td>
<td>2 V</td>
<td>4 V</td>
<td>6 V</td>
</tr>
</tbody>
</table>

(C) (2 points) Fill in the Q-device’s truth table below.

<table>
<thead>
<tr>
<th>Input Symbol</th>
<th>Output Symbol</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
</tr>
</tbody>
</table>
(D) (4 points) Specify the range of valid input voltages for each quaternary symbol that maximize noise immunity for the Q-device. What is its noise immunity?

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Valid input voltages</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>$V_{in} \leq ________$</td>
</tr>
<tr>
<td>1</td>
<td>$________&lt; V_{in} \leq ________$</td>
</tr>
<tr>
<td>2</td>
<td>$________&lt; V_{in} \leq ________$</td>
</tr>
<tr>
<td>3</td>
<td>$V_{in} &gt; ________$</td>
</tr>
</tbody>
</table>

Noise Immunity = __________

![Q-device VTC (repeated)](chart.png)
Problem 4. Combinational Logic (28 points)

(A) (5 points) The following BSV function \( f \) performs a basic operation using \( a \) and \( b \). We want \( f_2 \) to implement the same function as \( f \). Fill in the blank in \( f_2 \) to make the two functions equivalent. Write a single-line expression that uses the ternary operator (?:).

```hscl
function Bit#(n) f(Bit#(n) a, Bit#(1) b);
    Bit#(n) x = 0;
    for (Integer i = 0 ; i < valueOf(n) ; i = i+1) begin
        x[i] = a[i] ^ b;
    end
    return x;
endfunction

function Bit#(n) f2(Bit#(n) a, Bit#(1) b);
    return (     ___       ) ?     __       :       _        ;
endfunction
```

(B) (5 points) Write the truth table for the combinational device described by the function below.

```hscl
function Bit#(2) f(Bit#(1) a, Bit#(1) b, Bit#(1) c);
    Bit#(2) ret = zeroExtend(a) + signExtend(b);
    case ({a,b})
        0: ret = {1, c};
        2: ret = {a ^ b, a & b};
        3: ret = ~signExtend(c);
    endcase
    return ret;
endfunction
```

<table>
<thead>
<tr>
<th>a</th>
<th>b</th>
<th>c</th>
<th>ret[1]</th>
<th>ret[0]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td></td>
<td></td>
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<tr>
<td>0</td>
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<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
(C) (5 points) The following BSV function \( g \) performs a specific arithmetic operation on \( n \)-bit operands \( a \) and \( b \). We want the function \( g_2 \) to implement \( g \) in a single line of code. Fill in the blank with a single expression to make \( g_2 \) equivalent to \( g \).

```bsv
function Bit#(1) g(Bit#(n) a, Bit#(n) b);
    Bit#(2) ret = 'b10;
    for (Integer i = valueOf(n)-1 ; i > 0 ; i = i-1) begin
        if ({a[i], b[i]} == 'b01) ret = {0, ret[1] | ret[0]};
        else if ({a[i], b[i]} == 'b10) ret = {0, ret[0]};
    end
    return ret[1] | ret[0];
endfunction
```

```bsv
function Bit#(1) g2(Bit#(n) a, Bit#(n) b);
    return __________________________________________;
endfunction
```

(D) (5 points) Finish the following circuit diagram to implement function \( \text{computeB} \), given below. You may only use 32-bit 2-to-1 multiplexers, constants (0, 1, 2, 3, ...) and logic gates (AND, NOT, OR, XOR). We have provided three 32-bit greater-than-or-equal (\( \geq \)) comparators for you.

```bsv
function Bit#(32) computeB(Bit#(32) in);
    Bit#(32) out = 0;
    if ( in >= 1 ) out = 1;
    if ( in >= 5 ) out = 5;
    if ( in >= 10 ) out = 10;
    return out;
endfunction
```
(E) (8 points) Show that one-bit comparators can be used to implement any combinational circuit by implementing an inverter, an AND gate, and an OR gate using only comparator gates. You may tie inputs to 1 or 0 if necessary, and may use one or multiple comparator gates. Clearly label all inputs and outputs.

Logic diagram of inverter implementation using one-bit comparators:

\[
E_Q = A^\lor B \quad (A \text{ equals } B)
\]

\[
L_T = \overline{A} \cdot B \quad (A \text{ less than } B)
\]

Logic diagram of AND gate implementation using one-bit comparators:

Logic diagram of OR gate implementation using one-bit comparators:
Problem 5. Sequential logic timing (12 points)

You are given the sequential circuit shown below together with the timing parameters for each of the circuit elements in the table next to it.

![Sequential Circuit Diagram]

<table>
<thead>
<tr>
<th>Component</th>
<th>$t_{CD}$</th>
<th>$t_{PD}$</th>
<th>$t_{SETUP}$</th>
<th>$t_{HOLD}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>INV</td>
<td>20ps</td>
<td>100ps</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>AND</td>
<td>30ps</td>
<td>200ps</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>XOR</td>
<td>40ps</td>
<td>400ps</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>DREG</td>
<td>100ps</td>
<td>300ps</td>
<td>80ps</td>
<td>?ps</td>
</tr>
</tbody>
</table>

As is our convention for clocked devices, all timing specs for registers ($t_{CD}$, $t_{PD}$, $t_{SETUP}$, and $t_{HOLD}$) are measured relative to the rising edge of the clock.

(A) (4 points) Using the timing specifications in the table above, determine the minimum clock period required for this sequential circuit to work properly.

Minimum clock period for correct operation: __________ps

(B) (3 points) What is the propagation delay $t_{PD}$ for the output, OUT, of this sequential circuit relative to the rising edge of the clock?

$t_{PD}$: __________ps

(C) (5 points) What is the maximum value of $t_{HOLD}$ for the D registers to ensure that this circuit will work correctly? You may assume that $in = 0$ for this question.

Maximum value for $t_{HOLD}$ for correct operation: __________ps
Problem 6. Sequential Logic in BSV (24 points)

The following code implements a simple sequential circuit as a module that computes a function over a series of steps. Read the code and answer the questions about it below.

```haskell
interface Foo;
    method Action start(Bit#(32) aIn);
    method ActionValue#(Bit#(32)) getX();
    method Bit#(32) getI();
endinterface

module mkFoo(Foo);
    Reg#(Bit#(32)) a <- mkReg(0);
    Reg#(Bit#(1)) validx <- mkReg(0);
    Reg#(Bit#(32)) x <- mkRegU();
    Reg#(Bit#(32)) i <- mkRegU();

    function Bit#(32) computeB(Bit#(32) in);
        Bit#(32) out = 0;
        if ( in >= 1 ) out = 1;
        if ( in >= 5 ) out = 5;
        if ( in >= 10 ) out = 10;
        return out;
endfunction

    rule doComputeStep if (a > 0 && validx == 0);
        let b = computeB(a);
        a <= a - b;
        x <= a;
        validx <= 1;
        i <= i + 1;
endrule

    method Action start(Bit#(32) aIn) if (a==0);
        a <= aIn;
        i <= 0;
endmethod

    method ActionValue#(Bit#(32)) getX() if (validx == 1);
        validx <= 0;
        return x;
endmethod

    method Bit#(32) getI() if (a==0);
        return i;
endmethod
endmodule
```

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(A) (8 points) The module using mkFoo is invoking all the methods of mkFoo at every clock cycle. Remember that an invoked method can only execute when it is ready. The register values at the beginning of t0 is given. Fill the register values at the beginning of the following four clock cycles in the table below.

<table>
<thead>
<tr>
<th>time value</th>
<th>t0</th>
<th>t1</th>
<th>t2</th>
<th>t3</th>
<th>t4</th>
</tr>
</thead>
<tbody>
<tr>
<td>a</td>
<td>17</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>validx</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>x</td>
<td>27</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>i</td>
<td>3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(B) (4 points) The module using mkFoo is invoking the `getX` method of mkFoo at every clock cycle. Remember that an invoked method can only execute when it is ready. If the `start` method is called the first time with `aIn = 28`, what will the output sequence from `getX()`? What is the output of `getI()` after the `start` method is called?

1. Return value sequence of `getX()`:

2. Return value of `getI()`:

(C) (2 points) Suppose we get rid of register `x` and modify the rule `doComputeStep` and method `getX` as follows.

```
rule doComputeStep if (a > 0 && validx == 0);
  let b = computeB(a);
  a <= a - b;
  x <= a;
  validx <= 1;
  i <= i + 1;
endrule

method ActionValue#(Bit#(32)) getX() if (validx == 1);
  validx <= 0;
  return x;
  return a;
endmethod
```

Does this change the output sequence of `getX()` of the module?

(circle one) Yes ... No ... Can’t tell
(D) (2 points) Ignoring the changes in (C), suppose we modify the guard of `start` in the original code to `(a==0 && validx == 0)`. Does this change the output sequence of `getX()`?

(circle one)  Yes  ...  No  ...  Can’t tell

(E) (8 points) A partial circuit diagram for the implementation of `mkFoo` is given below.

Give the Boolean expressions for each write enable signal of registers a, `validx`, x, and i. You may use only wire names from the picture (e.g., t1, t2, ..., t9, `start.en`, `getX.en`, a, `validx`, x, i) and at most a total of three `AND(·)`, `OR(+)`, or `NOT(¬)` gates across all expressions.

\[ a.en : \quad \text{________________________} \]
\[ validx.en : \quad \text{________________________} \]
\[ x.en : \quad \text{________________________} \]
\[ i.en : \quad \text{________________________} \]

END OF QUIZ 1!