Virtual Memory
Goals of OS:
- Protection and privacy: Processes cannot access each other’s data
- Abstraction: Hide away details of underlying hardware
  - e.g., processes open and access files instead of issuing raw commands to hard drive
- Resource management: Controls how processes share hardware resources (CPU, memory, disk, etc.)
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Key enabling technologies:
Reminder: Operating Systems

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  - Interrupts to safely transition into supervisor mode
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Last lecture

Today
Virtual Memory (VM) Systems

*Illusion of a large, private, uniform store*

- Protection & Privacy
  - Each process has a private address space
Virtual Memory (VM) Systems

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- Demand Paging
Virtual Memory (VM) Systems

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Virtual Memory (VM) Systems

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- **Protection & Privacy**
  - Each process has a private address space

- **Demand Paging**
  - Use main memory as a cache of disk
  - Enables running programs larger than main memory
  - Hides differences in machine configuration
Virtual Memory (VM) Systems

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The price of VM is address translation on each memory reference
Names for Memory Locations

- Virtual address
  - Address generated by the process
  - Specific to the process’s private address space

- Physical address
  - Address used to access physical (hardware) memory
  - Operating system specifies mapping of virtual addresses into physical addresses
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Segmentation or Paging
Segmentation (Base-and-Bound) Address Translation

Process Address Space

0x0 to 0x0fff

Physical Memory

0x0 to 0xf..ff
Each program’s data is allocated in a contiguous segment of physical memory.
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Segmentation (Base-and-Bound) Address Translation

- Each program’s data is allocated in a contiguous segment of physical memory
- Physical address = Virtual Address + Segment Base
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0x0 to 0xf..ff

Process Address Space

0x0

Virtual Address

0x0fff

Physical Memory

0x0

Process Code & Data

Base Reg

+
Each program’s data is allocated in a contiguous segment of physical memory.

Physical address = Virtual Address + Segment Base

Bound register provides safety and isolation.
Each program’s data is allocated in a contiguous segment of physical memory
- Physical address = Virtual Address + Segment Base
- Bound register provides safety and isolation
- Base and Bound registers should not be accessed by user programs (only accessible in supervisor mode)
Separate Segments for Code and Data

Load X

Program Address Space

Data Bound Register
Virtual Address
Data Base Register

Main Memory

data segment

Code Bound Register
Program Counter
Code Base Register

code segment

Bounds Violation?

Bounds Violation?
Separate Segments for Code and Data

Pros of this separation?

Load X

Program Address Space

Data Bound Register

Virtual Address

Data Base Register

Bounds Violation?

Main Memory

data segment

code segment

Code Bound Register

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Program Counter

Code Base Register

Bounds Violation?

+
Separate Segments for Code and Data

Pros of this separation?
Prevents buggy program from overwriting code
Pros of this separation?

Prevents buggy program from overwriting code

Multiple processes can share code segment
Memory Fragmentation

- proc 1: 16K
- proc 2: 24K, 24K, 24K
- proc 3: 32K, 24K

OS Space

free
Memory Fragmentation

Processes 4 & 5 start

OS Space

proc 1
16K

proc 2
24K
24K
24K

proc 3
32K
24K

free
Memory Fragmentation

- OS Space
- proc 1: 16K
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Processes 4 & 5 start

free
Memory Fragmentation

Processes 4 & 5 start

OS Space

proc 1
16K
proc 2
24K
proc 3
24K
proc 4
16K
proc 5
8K
proc 3
32K
proc 5
24K

OS Space

proc 1
16K
proc 2
24K
proc 4
16K
proc 3
32K
proc 5
24K

free
Memory Fragmentation

Processes 4 & 5 start

Processes 2 & 5 end

OS Space

- proc 1: 16K
- proc 2: 24K
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- proc 5: 24K

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proc 2
proc 3
proc 4
proc 5

free
Memory Fragmentation

Processes 4 & 5 start

Processes 2 & 5 end

OS Space

proc 1 16K
proc 2 24K
proc 3 24K
proc 4 16K
proc 5 24K
proc 1 16K
proc 2 24K
proc 3 32K
proc 4 16K
proc 5 24K
proc 1 16K
proc 2 24K
proc 3 32K
proc 4 16K
proc 5 24K

free
As processes start and end, storage is “fragmented”. Therefore, at some point segments have to be moved around to compact the free space.
Paged Memory Systems

- Divide physical memory in fixed-size blocks called pages
  - Typical page size: 4KB
Paged Memory Systems

- Divide physical memory in fixed-size blocks called **pages**
  - Typical page size: 4KB

- Interpret each virtual address as a pair `<virtual page number, offset>`
Paged Memory Systems

- Divide physical memory in fixed-size blocks called **pages**
  - Typical page size: 4KB

- Interpret each virtual address as a pair `<virtual page number, offset>`

- Use a **page table** to translate from virtual to physical page numbers
  - Page table contains the physical page number (i.e., starting physical address) for each virtual page number
Private Address Space per Process

- Each process has a page table
- Page table has an entry for each process page
Private Address Space per Process

- Each process has a page table
- Page table has an entry for each process page

Page tables make it possible to store the pages of a program non-contiguously
Paging vs. Segmentation

Pros of paging vs segmentation?
Paging vs. Segmentation

Pros of paging vs segmentation?

Paging avoids fragmentation issues
Paging vs. Segmentation

Pros of paging vs segmentation?

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Paging vs. Segmentation

*Pros of paging vs segmentation?*

Paging avoids fragmentation issues

Paging allows programs that use more virtual memory than the machine’s physical memory (demand paging)
Paging vs. Segmentation

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Page tables are MUCH larger than base & bound regs!
Paging vs. Segmentation

_Pros of paging vs segmentation?_

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Paging allows programs that use more virtual memory than the machine’s physical memory (demand paging)

__Cons of paging vs segmentation?__

Page tables are MUCH larger than base & bound regs!

...where do we store the page tables?
Suppose Page Tables reside in memory.
Suppose Page Tables reside in memory

Virtual Page Number

VPN  offset  PT Base Reg

Kernel PT Base

PTB Proc $i$

PT Proc 1

PT Proc 2

Kernel PT
Suppose Page Tables reside in memory
Suppose Page Tables reside in memory

VPN | offset
---|---
PT Base Reg

Virtual Page Number

Kernel PT Base

Physical Page Number

Physical Base

PT Proc 1

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PT Proc i
Suppose Page Tables reside in memory
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- **Translation:**
  - $\text{PPN} = \text{Mem}[\text{PT Base} + \text{VPN}]$
  - $\text{PA} = \text{PPN} + \text{offset}$
Suppose Page Tables reside in memory

- Translation:
  - \( \text{PPN} = \text{Mem}[\text{PT Base} + \text{VPN}] \)
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- All links represent physical addresses; no VA to PA translation
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  - PPN = Mem[PT Base + VPN]
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- On process switch
  - PT Base Reg := Kernel PT Base + new process ID
Suppose Page Tables reside in memory

- Translation:
  - PPN = Mem[PT Base + VPN]
  - PA = PPN + offset
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  - PT Base Reg := Kernel PT Base + new process ID

Accessing one data word or instruction requires two DRAM accesses!
Demand Paging
Using main memory as a cache of disk

- All the pages of the processes may not fit in main memory. Therefore, DRAM is backed up by swap space on disk.
- Page Table Entry (PTE) contains:
Demand Paging

*Using main memory as a cache of disk*

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  - **DPN** (disk page number) for a page on the disk
  - Protection and usage bits
Demand Paging  
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  - Protection and usage bits
- Even if all pages fit in memory, demand paging allows bringing only what is needed from disk
  - When a process starts, all code and data are on disk; bring pages in as they are accessed
Example: Virtual → Physical Translation

Setup:
- 256 bytes/page (2^8)
- 16 virtual pages (2^4)
- 8 physical pages (2^3)
- 12-bit VA (4 vpn, 8 offset)
- 11-bit PA (3 ppm, 8 offset)

lw 0x2C8(x0)
VA = 0x2C8, PA = ________

VPN  offset
4 8  
3 8  

VA  PA

VPN  offset
0 0  
0 0  
0 1  
7 8  

Example: Virtual \(\rightarrow\) Physical Translation

<table>
<thead>
<tr>
<th>Page Table</th>
<th>Phys. Mem.</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>VPN 0x4</td>
</tr>
<tr>
<td>1</td>
<td>VPN 0x5</td>
</tr>
<tr>
<td>2</td>
<td>VPN 0x0</td>
</tr>
<tr>
<td>3</td>
<td>VPN 0xF</td>
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<tr>
<td>4</td>
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<tr>
<td>5</td>
<td>VPN 0xE</td>
</tr>
<tr>
<td>6</td>
<td>VPN 0xD</td>
</tr>
<tr>
<td>7</td>
<td>VPN 0xC</td>
</tr>
<tr>
<td>8</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td></td>
</tr>
<tr>
<td>A</td>
<td></td>
</tr>
<tr>
<td>B</td>
<td></td>
</tr>
<tr>
<td>C</td>
<td></td>
</tr>
<tr>
<td>D</td>
<td></td>
</tr>
<tr>
<td>E</td>
<td></td>
</tr>
<tr>
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<td></td>
</tr>
</tbody>
</table>

**16-entry Page Table**

**8-page Phys. Mem.**

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Example: Virtual $\rightarrow$ Physical Translation

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<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>2</td>
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<tr>
<td>1</td>
<td>--</td>
<td>--</td>
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<td>--</td>
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<td>0</td>
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<tr>
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<td>1</td>
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</tr>
<tr>
<td>F</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>3</td>
</tr>
</tbody>
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<p>| | | | | |</p>
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<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>VPN 0x4</td>
<td>0x000</td>
<td>0x0FC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VPN 0x5</td>
<td>0x100</td>
<td>0x1FC</td>
<td></td>
<td></td>
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<tr>
<td>VPN 0xF</td>
<td>0x300</td>
<td>0x3FC</td>
<td></td>
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</tr>
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<td>0x400</td>
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<td>0x600</td>
<td>0x6FC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VPN 0xC</td>
<td>0x700</td>
<td>0x7FC</td>
<td></td>
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$\text{lw} \ 0x2C8(x0)$
VA = 0x2C8, PA = ________
VPN = 0x2
Example: Virtual $\rightarrow$ Physical Translation

16-entry Page Table

|   | 0  | 0  | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | A  | B  | C  | D  | E  | F  |
|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 0 | 0  | 0  | 1  | 2  |    |    |    |    |    |    |    |    |    |    |    |    |
| 1 |    |    |    |    | 0  |    |    |    |    |    |    |    |    |    |    |    |
| 2 | 0  | 0  | 1  | 4  |    |    |    |    |    |    |    |    |    |    |    |    |
| 3 |    |    |    |    | 0  |    |    |    |    |    |    |    |    |    |    |    |
| 4 | 0  | 0  | 1  | 0  |    |    |    |    |    |    |    |    |    |    |    |    |
| 5 | 1  | 1  | 1  | 1  |    |    |    |    |    |    |    |    |    |    |    |    |
| 6 |    |    |    |    | 0  |    |    |    |    |    |    |    |    |    |    |    |
| 7 |    |    |    |    | 0  |    |    |    |    |    |    |    |    |    |    |    |
| 8 |    |    |    |    | 0  |    |    |    |    |    |    |    |    |    |    |    |
| 9 |    |    |    |    | 0  |    |    |    |    |    |    |    |    |    |    |    |
| A |    |    |    |    | 0  |    |    |    |    |    |    |    |    |    |    |    |
| B |    |    |    |    | 0  |    |    |    |    |    |    |    |    |    |    |    |
| C | 1  | 1  | 1  | 7  |    |    |    |    |    |    |    |    |    |    |    |    |
| D | 1  | 1  | 1  | 6  |    |    |    |    |    |    |    |    |    |    |    |    |
| E | 1  | 1  | 1  | 5  |    |    |    |    |    |    |    |    |    |    |    |    |
| F | 0  | 1  | 1  | 3  |    |    |    |    |    |    |    |    |    |    |    |    |


<table>
<thead>
<tr>
<th>VPN</th>
<th>offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x4</td>
<td>8</td>
</tr>
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→ PPN = 0x4
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Example: Virtual $\rightarrow$ Physical Translation

lw 0x2C8(x0)

VA = 0x2C8, PA = 0x4C8

VPN = 0x2

$\rightarrow$ PPN = 0x4
Caching vs. Demand Paging

**Caching**
- cache entry
- cache block (~32 bytes)
- cache miss rate (1% to 20%)
- cache hit (~1 cycle)
- cache miss (~100 cycles)
- a miss is handled in *hardware*

**Demand paging**
- page frame
- page (~4K bytes)
- page miss rate (<0.001%)
- page hit (~100 cycles)
- page miss (~5M cycles)
- a miss is handled mostly in *software*
Page Faults

An access to a page that does not have a valid translation causes a page fault exception. OS page fault handler is invoked, handles miss:

- Choose a page to replace, write it back if dirty. Mark page as no longer resident.
Page Faults

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- Read page from disk into available physical page
- Update page table to show new page is resident
- Return control to program, which re-executes memory access
Translation Lookaside Buffer (TLB)

Problem: Address translation is very expensive! Each reference requires accessing page table

Solution: *Cache translations in TLB*

- TLB hit ⇒ *Single-cycle translation*
- TLB miss ⇒ *Access page table to refill TLB*

---

**Diagram:**

```
<table>
<thead>
<tr>
<th>V</th>
<th>R</th>
<th>W</th>
<th>D</th>
<th>tag</th>
<th>PPN</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```

- virtual address
- (VPN = virtual page number)
- (PPN = physical page number)

```
<table>
<thead>
<tr>
<th>VPN</th>
<th>offset</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```

- physical address
- PPN
- offset

```
<table>
<thead>
<tr>
<th>fault?</th>
<th>hit?</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```

November 7, 2019

MIT 6.004 Fall 2019
Example: TLB and Page Table

Suppose
- Virtual memory of $2^{32}$ bytes
- Physical memory of $2^{24}$ bytes
- Page size is $2^{10}$ (1 K) bytes
- 4-entry fully associative TLB

1. How many pages can be stored in physical memory at once?
2. How many entries are there in the page table?
3. How many bits per entry in the page table? (Assume each entry has PPN, resident bit, dirty bit)
4. How many pages does page table take?
5. What is the physical address for virtual address 0x1804? What components are involved in the translation?
6. Same for 0x1080
7. Same for 0x0FC
Suppose

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- Physical memory of $2^{24}$ bytes
- Page size is $2^{10}$ (1 K) bytes
- 4-entry fully associative TLB

1. How many pages can be stored in physical memory at once? $2^{14}$

2. How many entries are there in the page table?

3. How many bits per entry in the page table? (Assume each entry has PPN, resident bit, dirty bit)

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Example: TLB and Page Table

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1. How many pages can be stored in physical memory at once? $2^{14}$
2. How many entries are there in the page table? $2^{22}$
3. How many bits per entry in the page table? (Assume each entry has PPN, resident bit, dirty bit)
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<thead>
<tr>
<th>VPN</th>
<th>V</th>
<th>R</th>
<th>D</th>
<th>PPN</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>7</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>9</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>0</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>0</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>0</td>
<td>0</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>1</td>
<td>0</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td></td>
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</tbody>
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<tbody>
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<td>0</td>
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7. Same for 0x1080

8. Same for 0x0FC
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TLB Designs

- Typically 32-128 entries, 4 to 8-way set-associative
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  - Page faults are always handled in software
  - But page walks are usually handled in hardware using a memory management unit (MMU)
    - RISC-V, x86 access page table in hardware
Address Translation

*Putting it all together*

Virtual Address

1. **TLB Lookup**
   - **hit**
   - **miss**

   - **Page Table Lookup**
     - the page is
     - memory
     - not memory

   - **Page Fault** (OS loads page)
     - Resume process at faulting instruction
   - **Update TLB**

   - **Protection Check**
     - permitted
     - denied

   - **Protection Fault**
     - Physical Address *(to mem)*

   - **SEGFAULT**
Using Caches with Virtual Memory

Virtually-Addressed Cache

- FAST: No virtual→physical translation on cache hits
- Problem: Must flush cache after context switch
Using Caches with Virtual Memory

Virtually-Addressed Cache

- FAST: No virtual→physical translation on cache hits
- Problem: Must flush cache after context switch

Physically-Addressed Cache

- Avoids stale cache data after context switch
- SLOW: Virtual→physical translation before every cache access
Best of Both Worlds: Virtually-Indexed, Physically-Tagged Cache (VIPT)

OBSERVATION: If cache index bits are a subset of page offset bits, tag access in a physical cache can be done *in parallel* with TLB access. Tag from cache is compared with physical page address from TLB to determine hit/miss.
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Cache index comes entirely from address bits in page offset – don’t need to wait for TLB to start cache lookup!
Best of Both Worlds: Virtually-Indexed, Physically-Tagged Cache (VIPT)

OBSERVATION: If cache index bits are a subset of page offset bits, tag access in a physical cache can be done in parallel with TLB access. Tag from cache is compared with physical page address from TLB to determine hit/miss.

Problem: Limits # of bits of cache index → can only increase cache capacity by increasing associativity!
Summary

- Virtual memory benefits:
  - Protection and privacy: Private address space per process
  - Demand paging: Can use main memory as a cache of disk
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  - Protection and privacy: Private address space per process
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  - Simple: Base and bound registers
  - Suffers from fragmentation, no demand paging

- Paging: Each process address space is stored on multiple fixed-size pages. A page table maps virtual to physical pages
  - Avoids fragmentation
  - Enables demand paging: pages can be in main memory or disk
  - Requires a page table access on each memory reference

- TLBs make paging efficient by caching the page table
Thank you!

Next lecture: Pipelined Processors