Note: A small subset of essential problems are marked with a red star (★). We especially encourage you to try these out before recitation.
Problem 1. ★

Ms. Anna Logge, founder at a local MIT startup, has developed a device to be used as an inverter. Anna is considering the choice of parameters by which her logic family will represent logic values and needs your help.

The figure on the right shows the voltage transfer curve of a proposed inverter for a new logic family (you can find spare copies below).

Several possible schemes for mapping logic values to voltages are being considered, as summarized in the incomplete table below. Noise Immunity (the last row) is defined as the smaller of the two noise margins.

Complete the table by filling in missing entries. Choose each value to maximize the noise margins of the corresponding scheme. If the numbers in a scheme can’t be completed such that the device functions as an inverter with positive noise margins, fill the entries for that column with Xs.

LNI’s Possible Logic Mappings:

<table>
<thead>
<tr>
<th>Scheme</th>
<th>Scheme A</th>
<th>Scheme B</th>
<th>Scheme C</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{OL} )</td>
<td>X</td>
<td>0.5</td>
<td>1</td>
</tr>
<tr>
<td>( V_{IL} )</td>
<td>2</td>
<td>1</td>
<td>0.5</td>
</tr>
<tr>
<td>( V_{IH} )</td>
<td>X</td>
<td>3</td>
<td>X</td>
</tr>
<tr>
<td>( V_{OH} )</td>
<td>X</td>
<td>5</td>
<td>X</td>
</tr>
<tr>
<td>Noise Immunity</td>
<td>X</td>
<td>0.5</td>
<td>X</td>
</tr>
</tbody>
</table>

\[ V_{OUT} \]

\[ V_{IN} \]
Scheme A: illegitimate, \( V_{IL} = 2 \) places the “trough” part of the VTC within the “valid input” range; however, since the trough touches the horizontal axis (\( V_{OUT} = 0 \)), any choice for \( V_{OL} \) will cause the VTC to overlap with a forbidden region.

Scheme B: \( V_{OL} = 0.5, V_{OH} = 5 \). Noise Immunity = 0.5. The values of \( V_{IL} = 1 \) and \( V_{IH} = 3 \) exclude the jagged part of the VTC from consideration. Thus, we simply set \( V_{OL} = 0.5 \) (the value of \( V_{OUT} \) for \( V_{IN} > 3 \)) and set \( V_{OH} = 5 \) (the value of \( V_{OUT} \) for \( V_{IN} < 1 \)) to maximize our noise margins. We calculate our noise immunity as:

\[
\text{Noise Immunity} = \min(5-3, 1-0.5) = 0.5
\]

Scheme C: illegitimate, since \( V_{OL} < V_{IL} < V_{IH} < V_{OH} \) must hold for a legitimate specification.
Problem 2.

Suppose that you measured the voltage transfer curve of the device shown below. Can we find a signaling specification \((V_{IL}, V_{IH}, V_{OL}, V_{OH})\) that would allow this device to be a digital inverter? If so, give the specification that maximizes noise margin.

Note: Noise Margin = \(\min(\text{Low Noise Margin, Max Noise Margin})\)

In general, we can solve these optimization problems for simple, step-wise VTC curves by choosing the most extreme values for \(V_{OH}\) and \(V_{OL}\) (i.e. maximizing \(V_{OH} - V_{OL}\) ) and moving those lines more centrally until we have legitimate specifications. Often, we will discover constraints that define a strict relationship between the aforementioned output voltages and the input voltages \(V_{IH}\) and \(V_{IL}\); thus, selecting optimal \(V_{OH}\) and \(V_{OL}\) imply an optimal \(V_{IH}\) and \(V_{IL}\) in these cases. Here is an example of how you might optimize:

Iteration 1: \(V_{OL} = 0.5, V_{OH} = 5 \Rightarrow V_{IL} = 0, V_{IH} = 3\)
(illegitimate because \(V_{IL} = 0\) is impossible)

Iteration 2: \(V_{OL} = 0.5, V_{OH} = 4 \Rightarrow V_{IL} = 1, V_{IH} = 3\)
(legitimate; yields a Low Noise Margin of \(1 - 0.5 = 0.5\) and a High Noise Margin of \(4 - 3 = 1\))

At this point, we notice that the limiting factor in maximizing the Noise Margin is the Low Noise Margin. Thus, since we cannot decrease \(V_{OL}\) any further, we must increase \(V_{IL}\) to optimize. However, notice that increasing further implies a decrease in order to keep the VTC outside of the forbidden regions. Thus, we will eventually reach an equilibrium at which the noise margins are equal:

\[ V_{OH} - V_{IH} = V_{IL} - V_{OL} \]

Noting that the optimal point \((V_{IL}, V_{OH})\) lies in the middle segment of the graph and that this segment has slope \((1-4)/(2.5-1) = -2\), we have:

\[ V_{OH} = 4 - 2(V_{IL} - 1) \]
\[ 4 - 2(V_{IL} - 1) - 3 = V_{IL} - 0.5 \Rightarrow V_{IL} = 7/6 \Rightarrow V_{OH} = 4 - 2(7/6 - 1) = 11/3 \]
Problem 3. ⭐

Suppose we define all signaling thresholds in our digital system to be relative to the supply voltage, \( V_{DD} \):
- \( V_{OL} = 0.1 V_{DD} \)
- \( V_{IL} = 0.4 V_{DD} \)
- \( V_{IH} = 0.6 V_{DD} \)
- \( V_{OH} = 0.9 V_{DD} \)

We want to connect two types of digital devices, A and B, that use different supply voltages, \( V_{DD,A} \) and \( V_{DD,B} \). **Assume that \( V_{DD,A} = 1V \).**

(1) In the circuit below, under what range of supply voltages \( V_{DD,B} \) will the system work correctly?

(2) In the circuit below, under what range of supply voltages \( V_{DD,B} \) will the system work correctly?

(3) For the same circuit as in part 2, under what range of supply voltages \( V_{DD,B} \) will the system have noise margins of at least 0.1V?
Problem 4. ★

The following are voltage transfer characteristics of single-input, single-output devices to be used in a new logic family:

![Voltage Transfer Characteristics Diagram]

Your job is to choose a single set of signaling thresholds $V_{OL}$, $V_{IL}$, $V_{OH}$, and $V_{IH}$ to be used with both devices to give the best noise margins you can. Recall that the VTC can touch the edge of the forbidden regions but not pass through those regions. Fill in your answers below, together with the resulting noise margins. You’ll get partial credit for anything that works with nonzero noise margins; for full credit, maximize the noise immunity (i.e., the smaller of the two noise margins).

\[
\begin{align*}
V_{OL} &= \underline{0.5} \\
V_{IL} &= \underline{1.5-1.67} \\
V_{IH} &= \underline{3.5} \\
V_{OH} &= \underline{4.5} \\
\text{Low Noise Margin} &= \underline{1-1.17} \\
\text{High Noise Margin} &= \underline{1}
\end{align*}
\]
Note: Noise Margin = min(Low Noise Margin, Max Noise Margin)

As in Problem 1, we begin our optimization by choosing the most extreme values for \( V_{OH} \) and \( V_{OL} \) (i.e. maximizing \( V_{OH} - V_{OL} \)) and moving those lines more centrally until we have legitimate specifications. In this case, we must pay attention to the VTCs of two devices simultaneously. Here is an example of how you might optimize:

Iteration 1: \( V_{OL} = 0, V_{OH} = 5 \Rightarrow V_{IL} = 1.5, V_{IH} = 3 \)  
(illegitimate because \( V_{OL} = 0 \) is impossible; also, both VTCs overlaps forbidden regions)

Iteration 2: \( V_{OL} = 0.5, V_{OH} = 4.5 \Rightarrow V_{IL} = 1.5, V_{IH} = 3 \)  
(better, but still illegitimate because \( V_{IH} \) is too low)

Iteration 3: \( V_{OL} = 0.5, V_{OH} = 4.5 \Rightarrow V_{IL} = 1.5, V_{IH} = 3.5 \)  
(legitimate)

Graphically, we see that we cannot improve the High Noise Margin any further. However, for the sake of completeness, we can continue optimizing the Low Noise Margin.

Iteration 4: \( V_{OL} = 0.5, V_{OH} = 4.5 \Rightarrow V_{IL} = 1.67, V_{IH} = 3.5 \)  
(legitimate; we simply traced a horizontal line at \( V_{OH} = 4.5 \) to find where it intercepts Device A’s VTC. This point is the largest threshold for \( V_{IL} \) can achieve)

The answers to Iteration 3 and Iteration 4 are both acceptable, as they both have the minimum noise margin of 1.
Problem 5.

The following are voltage transfer characteristics of devices to be used in a new logic family as an inverter and buffer, respectively:

Your job is to choose a single set of signaling thresholds $V_{OL}$, $V_{IL}$, $V_{OH}$, and $V_{IH}$ to be used with both devices to give the best noise margins you can. Recall that the VTC can touch the edge of the forbidden regions but not pass through those regions. Fill in your answers below, together with the resulting noise margins. You’ll get partial credit for anything that works with nonzero noise margins; for full credit, maximize each of the noise margins.

$V_{OL} = \underline{1}$ $V_{IL} = \underline{1.5}$ $V_{IH} = \underline{3}$ $V_{OH} = \underline{4}$

Low Noise Margin = \underline{0.5} High Noise Margin = \underline{1}

Scratch copy of the VTC diagrams:
**Note:** Noise Margin = \( \min(\text{Low Noise Margin}, \text{Max Noise Margin}) \)

As in Problem 4, we begin our optimization by choosing the most extreme values for \( V_{\text{OH}} \) and \( V_{\text{OL}} \) (i.e. maximizing \( V_{\text{OH}} - V_{\text{OL}} \)) and moving those lines more centrally until we have legitimate specifications. Here is an example of how you might optimize:

**Iteration 1:** \( V_{\text{OL}} = 0, V_{\text{OH}} = 4.5 \Rightarrow V_{\text{IL}} = 0, V_{\text{IH}} = 5 \)
(illegitimate because \( V_{\text{OL}}, V_{\text{IL}} = 0 \) is impossible; also, VTC overlaps forbidden regions)

**Iteration 2:** \( V_{\text{OL}} = 0.5, V_{\text{OH}} = 4 \Rightarrow V_{\text{IL}} = 1.25, V_{\text{IH}} = 4 \)
(legitimate; we get \( V_{\text{IL}} = 1.25 \) and \( V_{\text{IH}} = 4 \) by drawing a horizontal line at \( V_{\text{OL}} = 0.5 \) and seeing where it intercepts the second and first VTCs, respectively)

At this point, we can calculate that the Low Noise Margin = 0.75 and the High Noise Margin = 0. Clearly, we need to increase the High Noise Margin to improve our overall result. Since we cannot increase our \( V_{\text{OH}} \), we must instead decrease our \( V_{\text{IH}} \), and we can afford to sacrifice the size of our Low Noise Margin to achieve this.

We increase \( V_{\text{OL}} \) by the smallest possible increment (0.5) in order to decrease our \( V_{\text{IH}} \) while keeping a legitimate specification.

**Iteration 3:** \( V_{\text{OL}} = 1, V_{\text{OH}} = 4 \Rightarrow V_{\text{IL}} = 1.5, V_{\text{IH}} = 3 \)
(legitimate and optimal; Low Noise Margin = 0.5 and High Noise Margin = 1)
Problem 6. ★

The voltage transfer curve for an inverter is shown to the right. The manufacturer decided to crowdsource the digital signaling specifications for their inverter and has received some suggestions for $V_{OL}$, $V_{IL}$, $V_{IH}$, and $V_{OH}$, presented in tabular form below.

For each suggested specification, determine if the inverter would be a legitimate combinational device with non-zero positive noise margins. If it is a legitimate combinational device, give the noise immunity of the inverter (the smaller of the low and high noise margins) when operating under that specification. If the inverter wouldn’t be a legitimate combinational device, please write NOT LEGIT in the rightmost column.

Fill in rightmost column for each suggested specification.

<table>
<thead>
<tr>
<th>Suggestion</th>
<th>$V_{OL}$</th>
<th>$V_{IL}$</th>
<th>$V_{IH}$</th>
<th>$V_{OH}$</th>
<th>Noise immunity, or NOT LEGIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>#1</td>
<td>0.00</td>
<td>0.50</td>
<td>1.50</td>
<td>2.00</td>
<td>Not legit</td>
</tr>
<tr>
<td>#2</td>
<td>0.25</td>
<td>0.75</td>
<td>1.25</td>
<td>1.75</td>
<td>Not legit</td>
</tr>
<tr>
<td>#3</td>
<td>0.50</td>
<td>0.75</td>
<td>1.25</td>
<td>1.50</td>
<td>0.25</td>
</tr>
<tr>
<td>#4</td>
<td>0.75</td>
<td>0.50</td>
<td>1.75</td>
<td>1.50</td>
<td>Not legit</td>
</tr>
</tbody>
</table>

#1: Can’t produce $V_{OL} = 0$ output

#2: Test: For $V_{in} \geq V_{IH} = 1.25$, is $V_{out} \leq V_{OL} = 0.25$? Not satisfied

#3: Valid:

#4: Test: Is $V_{OL} < V_{IL} < V_{IH} < V_{OH}$? Not satisfied
Problem 7. ★

The circuit C shown below is a 2-input, 2-output combinational device.

![Circuit C Diagram]

Each of the three circuits below contains multiple copies of circuit C. Note: the ▲ symbol indicates a “floating” input.

![Circuit 1 Diagram]

![Circuit 2 Diagram]

![Circuit 3 Diagram]

(A) Below is one possible implementation of C:

![Circuit C Alternative Diagram]

Given this implementation, determine which of the above circuits are combinational.

Circuit 1  Yes  Circuit 2  No  Circuit 3  Yes

(B) Below is an alternative implementation of C:

![Circuit C Alternative Diagram]

Given this alternative implementation, determine which of the above circuits are combinational.

Circuit 1  Yes  Circuit 2  Yes  Circuit 3  Yes
A) Circuit 1: This is combinational, which we can determine by tracing paths from the inputs to the outputs.

Circuit 2: This is not combinational, because the floating inputs may be invalid even when the original inputs to the circuit are valid, and since this floating inputs affect the outputs of the circuits, we may obtain invalid outputs even with valid inputs.

Circuit 3: This is combinational, which we can determine by tracing paths from the input to the output. In fact, this circuit simply copies its input to the output.

B) Circuit 1: This is combinational, which we can determine by tracing paths from the inputs to the outputs. In fact, this circuit simply copies its inputs to the output.

Circuit 2: This is combinational, which we can determine by tracing paths from the inputs to the outputs. In fact, this circuit simply copies its inputs to the outputs. Note that the floating inputs do not affect the outputs, which is why this circuit is still combinational despite their presence.

Circuit 3: This is combinational, which we can determine by tracing paths from the inputs to the outputs. In fact, this circuit simply inverts its input. Note that the directed cycle in this circuit stands alone and does not affect the output, which is why it is still combinational.
From past quizzes:

Problem 8. Static Discipline (13 points)

Consider the voltage transfer characteristic (VTC) of a hypothetical Device F shown below (not to scale). Ben Bitdiddle is considering two different choices for each of \(V_{OH}\) and \(V_{OL}\), as indicated by the dashed lines on the graph below. The precise values of these thresholds are listed in the table. \(V_{IL}\) is known to be 1.5V.

![Graph showing voltage transfer characteristic](image)

<table>
<thead>
<tr>
<th>Variable (V)</th>
<th>Value (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{OH,A})</td>
<td>4.7</td>
</tr>
<tr>
<td>(V_{OH,B})</td>
<td>4.2</td>
</tr>
<tr>
<td>(V_{OL,C})</td>
<td>1.8</td>
</tr>
<tr>
<td>(V_{OL,D})</td>
<td>1.0</td>
</tr>
<tr>
<td>(V_{IL})</td>
<td>1.5</td>
</tr>
</tbody>
</table>

(A) (4 points) \(V_{IH}\) is not known right now but is guaranteed to be between 3.0 V and 4.0 V. For each choice of \(V_{OH}\), circle YES if it both follows the static discipline and has a positive **high noise margin**, or circle NO if it does not satisfy both of these conditions. If the answer depends on knowing values that are not provided, then circle DON'T KNOW.

\(V_{OH,A}\) (circle one): **YES**  **NO**  **DON'T KNOW**

\(V_{OH,B}\) (circle one): **YES**  **NO**  **DON'T KNOW**

\(V_{OH,A}\): NO because 4.7 V is too high of a threshold for valid logic high levels given the current \(V_{IL}\). Observe that for certain values of \(V_{in} < V_{IL}\) (i.e. valid input low voltages), some values on the VTC fall below \(V_{OH,A}\). In other words, there are some valid low inputs that would produce invalid outputs.

\(V_{OH,B}\): YES because 4.2 V satisfies the static discipline and provides a positive high noise margin. For all input voltages below \(V_{IL}\), the output voltage of Device F is above \(V_{OH,B}\). That is to say, all valid input low voltages will produce valid output high voltages (which is required to follow the static discipline). Furthermore, the high noise margin with \(V_{OH,B}\) is computed with \(V_{OH,B} - V_{IH}\). Since 3.0 < \(V_{IH}\) < 4.0, the high noise margin must be positive.
(B) (4 points) For each choice of $V_{OL}$, circle YES if it both follows the static discipline and allows for a positive low noise margin, or circle NO if it does not satisfy both of these conditions. If the answer depends on knowing values that are not provided, then circle DON’T KNOW.

$V_{OL,C}$: NO because the low noise margin would be negative. The low noise margin is computed with $V_{IL} - V_{OL,C} = -0.3$ V.

$V_{OL,D}$: DON’T KNOW because even though the low noise margin is positive, we cannot say for sure if this value obeys the static discipline without knowing the exact value of $V_{IH}$.

$V_{OL,C}$ (circle one): YES NO DON’T KNOW

$V_{OL,D}$ (circle one): YES NO DON’T KNOW

(C) (2 points) Suppose Ben settles on the following signaling specification which follows the static discipline:

$V_{IL} = 1.5$ V
$V_{IH} = 3.8$ V
$V_{OL} = 1.4$ V
$V_{OH} = 4$ V

Calculate the high and low noise margins as well as the noise margins of the device as a whole.

High Noise Margin: ______________ 0.2 V

Low Noise Margin: ______________ 0.1 V

Overall Noise Margin: ______________ 0.1 V

High Noise Margin = $V_{OH} - V_{IH} = 4 - 3.8 = 0.2$ V
Low Noise Margin = $V_{IL} - V_{OL} = 1.5$ V $- 1.4$ V = 0.1 V
Overall Noise Margin = min{High Noise Margin, Low Noise Margin} = 0.1 V

(D) (3 points) Alyssa P. Hacker has another Device G with the following VTC that she would like to use with Device F. Can she use Device G with Device F and the signaling specifications described in part (C)? If she can, circle NO CHANGES. Otherwise, circle CHANGES NEEDED and change exactly one of the thresholds of the signaling specification to a new value such that Device G can be used while obeying the static discipline and maximizing noise margins. Also calculate the overall noise margin of the resulting system, regardless of whether or not you changed any thresholds. Keep in mind that VTCs may touch the edge of, but not enter the forbidden region.
The $V_{OH}$ used in Part (B) is too high. Device G only produces 3.9 V at input voltages above 3.8 V, the threshold for a valid logic high input. This is the only threshold that needs to be changed and changing no other threshold will solve this problem since the VTC is flat above 3.5 V on the input. Therefore, the threshold for what we consider to be a logic level high on the output side ($V_{OH}$) needs to be lowered to something at or below 3.9 V. We need to be careful though because lowering it too far will drop it below $V_{IH} = 3.8$ V which would cause a negative noise margin. In fact, we should set $V_{OH}$ to be exactly 3.9 to maximize noise margins. This would give a noise margin of 0.1 V.
From past quizzes:

Problem 9. Static Discipline (13 points)

The R module below outputs 0.5V when \( \min(V_A, 0.5V_B) > 2V \) for 25ns and outputs 6V when \( \min(V_A, 0.5V_B) < 1.5V \) for 25ns. This is summarized in the equation below (assume all voltages are positive). Also, assume this circuit obeys a digital signaling specification where low voltages correspond to digital 0 and high voltages correspond to digital 1.

\[
V_{out} = \begin{cases} 
0.5V, & \min(V_A, 0.5V_B) > 2V \\
6V, & \min(V_A, 0.5V_B) < 1.5V \\
0 \leq ??? \leq 6V, & \text{otherwise}
\end{cases}
\]

(A) (2 points) If we apply constant \( V_A, V_B \) for 25ns and then measure \( V_{out} = 0.5V \), what can we conclude about \( V_B \)?

- **C1**: \( V_B < 3V \)
- **C2**: \( V_B \leq 4V \)
- **C3**: \( V_B > 4V \)
- **C4**: \( V_B \geq 3V \)
- **C5**: None of the above

(label: 6A) Best conclusion about \( V_B \) (Select one): C1 ... C2 ... C3 ... C4 ... C5

We have no guarantees on the output voltage values when the input voltage is between 1.5V and 2V. The output voltage could come from an input voltage within this range or an input voltage where \( \min(V_A, 0.5V_B) > 2V \) holds. We know, however, it could not come from an input voltage where \( \min(V_A, 0.5V_B) < 1.5V \) holds. Otherwise, the output would be 6V. Thus, we know \( \min(V_A, 0.5V_B) \geq 1.5V \) is true. This means that \( V_B \geq 3 \).

(B) (3 points). What Boolean expression does R implement? Specify an equation using A and B.

A=1 (a high voltage) and B=1 (a high voltage) gets mapped to 0.5V, or 0. A=0 (a low voltage) and B=0 (a low voltage) gets mapped to 6V, or 1. A=1 and B=0 maps to the same value as A=0 and B=0, as the minimum is taken. Similarly, B=1 and A=0 maps to the same value as A=0 and B=0. Thus, this truth table describes the Boolean expression \( \overline{AB} \).

(label: 6B) Boolean Expression: \( \text{out}(A, B) = \underline{\phantom{0}} \overline{AB} \underline{\phantom{0}} \)
(C) (5 points) Find a signaling specification that maximizes noise immunity for the R module.

**Note:** Noise Margin = \( \min(\text{Low Noise Margin}, \text{Max Noise Margin}) \)

As before, we begin our optimization by choosing the most extreme values for \( V_{OH} \) and \( V_{OL} \) (i.e. maximizing \( V_{OH} - V_{OL} \)) and moving those lines more centrally until we have legitimate specifications. Thus, we set \( V_{OL} = 0.5 \) and \( V_{OH} = 6 \). If \( V_A < 1.5 \) and/or \( V_B < 3 \), then the output voltage is 6V. If \( V_A > 2 \) and/or \( V_B > 4 \), the output voltage is 0.5. This, if the voltage is less than 1.5, the output voltages is 6. If the voltage is greater than 4, the output voltage is 0.5. Then, we can set \( V_{IL} = 1.5, V_{IH} = 4 \).

Noise immunity = \( \min(1.5 - 0.5, 6 - 4) = 1 \)

\[
\text{(label: 6C_1)} \quad V_{OL} = 0.5, V_{IL} = 1.5, V_{IH} = 4, V_{OH} = 6
\]

\[
\text{(label: 6C_2)} \quad \text{Noise Immunity} = \quad 1 \quad \text{__________}
\]

(D) (3 points) Suppose one wishes to using the R module as an inverter, as shown below. What is the noise immunity of this device?

\[
V_{OL} = 0.5, V_{IL} = 3, V_{IH} = 4, V_{OH} = 6
\]

\[
\text{(label: 6D)} \quad \text{Noise Immunity: \quad 2 \quad \text{__________}}
\]