Problem 1

a) Fill in the conflict matrix for this design. You may assume that the fifo we’ve provided allows for concurrent calls to enq and deq.

b) Draw a hardware circuit for this design, ignoring the internals of the fifo design. Include the internals of the bluespec scheduler generated for this design.

c) Repeat the previous two parts, but this time you may assume that the fifo we’ve provided doesn’t allow for concurrent calls to enq and deq.

```plaintext
rule stage1;
    fifo.enq(f0(inQ.first));
inQ.deq;
endrule
rule stage2;
    outQ.enq(f1(fifo.first));
fifo.deq;
endrule
```
Problem 2

```plaintext
rule ra(p1);
  x <= y + 1;
endrule
rule rb(p2);
  y <= z + 2;
endrule
rule rc(p3);
  z <= x + 2;
endrule
```

a) Fill in the Conflict Matrix for this design.

b) Can all three rules execute concurrently?

c) Can any two rules execute concurrently?

Problem 3

a)