6.004 Tutorial Problems
L11 – Sequential Circuits in Minispec

**Note:** A subset of problems are marked with a red star (★). We especially encourage you to try these out before recitation.

**Problem 1. ★**
Implement the combination lock FSM from Lecture 10 as a Minispec module. The lock FSM should unlock only when the last four input bits have been 0110. The diagram below shows the FSM’s state-transition diagram.

(A) Implement this state-transition diagram by filling in the code skeleton below. Use the State enum to ensure state values can only be S0-S5.

```plaintext
typedef enum { S0, S1, S2, S3, S4 } State;

module Lock;
    Reg#(State) state(S0);
    input Bit#(1) in;

    rule tick;
        state <= case (state)
            S0:
            ______________________________;
            S1:
            ______________________________;
            S2:
            ______________________________;
            S3:
            ______________________________;
            S4:
            ______________________________;
        endcase;
    endrule

    method Bool unlock = ______________________________;
endmodule
```

![State Transition Diagram](image)
(B) How many flip-flops does this lock FSM require to encode all possible states?

(C) Consider an alternative implementation of the Lock module that stores the last four input bits. Fill in the skeleton code below to complete this implementation.

```verilog
module Lock;
    Reg#(Bit#(4)) lastFourBits(4'b1111);

    input Bit#(1) in;

    rule tick;
        lastFourBits <= _________________________________;
    endrule

    method Bool unlock = _________________________________;
endmodule
```
Problem 2. ★

Implement the Fibonacci FSM from Problem 3 of the previous worksheet by filling in the code skeleton below.

// Use 32-bit values
typedef Bit#(32) Word;

module Fibonacci;
    Reg#(Word) x(0);
    Reg#(Word) y(0);
    Reg#(Word) i(0);

    input Maybe#(Word) in default = Invalid;

    rule tick;

        method Maybe#(Word) result = ________________________________;
    endmethod

endrule

endmodule
Problem 3.

Implement a sequential circuit to compute the factorial of a 16-bit number.

(A) Design the circuit as a sequential Minispec module by filling in the skeleton code below. The circuit should start a new factorial computation when a Valid input is given. Register \texttt{x} should be initialized to the input argument, and register \texttt{f} should eventually hold the output. When the computation is finished, the result method should return a Valid result; while the computation is ongoing, result should return In\texttt{valid}.

You can use the multiplication operator (*). * performs unsigned multiplication of Bit\texttt{(n)} inputs. Assume inputs and results are unsigned. Though we have not yet seen how to multiply two numbers, lab 5 includes the design of a multiplier from scratch.

```minispec
module Factorial;
    Reg#(Bit#(16)) x(0);
    Reg#(Bit#(16)) f(0);

    input Maybe#(Bit#(16)) in default = Invalid;

    rule factorialStep;

    method Maybe#(Bit#(16)) result =
        __________________________________________;

endmodule
```

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(B) Manually synthesize your Factorial module into a sequential circuit with registers and combinational logic blocks (similar to how Lecture 11 does this with GCD). No need to draw the implementation of all basic signals (e.g., you can give formulas, like for the sel signal in Lecture 11).
Problem 4. Sequential Circuits in Minispec (Fall 2019 Quiz 2, Problem 3, 18 points)

You join a startup building hardware to mine Dogecoins. In this cryptocurrency, mining coins requires repeatedly evaluating a function with two arguments, \( sc(x, y) \). \( x \) is given to you, and mining requires trying different values of \( y \) until you find a \( y \) for which \( sc(x, y) \) is below a threshold value. Finding such a \( y \) value yields several Dogecoins as a reward, which you can then exchange for cold hard cash.

Because the \( sc \) function is expensive, it is implemented as a multi-cycle sequential module, called SC. SC is given to you. Its implementation is irrelevant, and its interface, shown below, is the usual interface for multi-cycle modules: SC has a single input, \( \text{in} \), and a single method, \( \text{getResult()} \). To start a new computation, the module user sets \( \text{in} \) to a \( \text{Valid Args} \) struct containing arguments \( x \) and \( y \). Some cycles later, SC produces the result as a \( \text{Valid} \) output of its \( \text{getResult()} \) method. While SC is processing an input, the \( \text{getResult()} \) method returns \( \text{Invalid} \) and \( \text{in} \) should stay \( \text{Invalid} \).

```verilog
module SC;
    input Maybe#(Args) in default = Invalid;
    typedef struct {
        Bit#(32) x;
        Bit#(32) y;
    } Args;

    method Maybe#(Bit#(32)) getResult();
        // unknown implementation
    endmethod

    // unknown rules
endmodule
```

You are asked to design the \( \text{ArgFeeder} \) module, which accepts an input \( x \), and feeds a sequence of inputs \( (x, 0), (x, 1), (x, 2), ..., (x, y-1), (x, y) \) to the SC module. \( \text{ArgFeeder} \) keeps feeding values to SC until SC’s result is less than \( \text{threshold} \) (a parameter to your module). At that point, \( \text{ArgFeeder} \) should return the \( y \) such that \( (x, y) \) meets this condition through its \( \text{getResult()} \) method. The diagram below sketches the implementation of \( \text{ArgFeeder} \). Like SC, \( \text{ArgFeeder} \) follows the usual interface for a multi-cycle module.

Implement the \( \text{ArgFeeder} \) module by completing the implementation of the \( \text{getResult()} \) method and the \( \text{tick} \) rule. The rule considers three cases:

(i) a new input is provided to \( \text{ArgFeeder} \),
(ii) SC returns a \( \text{Valid} \) result, and it is less than the threshold value, and
(iii) SC returns a \( \text{Valid} \) result, but it is not less than the threshold value.

You may use any Minispec operator, including arithmetic (+, -, *, /). You will not need additional registers to complete this problem. Do not add additional rules, methods, or functions.
module ArgFeeder#(Integer threshold);
  SC sc;

  Reg#(Maybe#(Bit#(32))) out(Invalid);
  RegU#(Bit#(32)) x;
  RegU#(Bit#(32)) y;

  input Maybe#(Bit#(32)) in_x default = Invalid;

  method Maybe#(Bit#(32)) getResult();
    // implement the getResult() method
    return ;
  endmethod

  rule tick;
    if (isValid(in_x)) begin
      // case (i): received a new input; start a new sequence of (x, y) pairs
      sc.in = Valid(Args{x: , y: });
      out <= ;
      x <= ;
      y <= ;
    end else if (isValid(sc.getResult())) begin
      if (fromMaybe(?, sc.getResult()) < threshold) begin
        // case (ii): result satisfies threshold
        out <= ;
      end else begin
        // case (iii): result does not yet satisfy threshold
        // send next (x, y) pair to SC
        sc.in = Valid(Args{x: , y: });
        y <= ;
      end
    end else begin
      // case (iii): result does not yet satisfy threshold
      // send next (x, y) pair to SC
      sc.in = Valid(Args{x: , y: });
      y <= ;
    end
  endrule
endmodule
Problem 5. Sequential Minispec (Spring 2020 Quiz 2, Problem 4, 16 points)

The incomplete Minispec module, `FindLongestBitRun`, below counts the length of the longest string of 1’s in a 32-bit word. The algorithm works by repeatedly performing a bitwise AND of the word with a version of itself that has been left-shifted by one. This repeats until the word is 0. The number of iterations required is the longest string of 1’s in the word. This works because each iteration converts the last 1 in any string of 1’s into a 0. The word will not equal zero until its longest string of 1’s has all been converted into 0’s.

The circuit should start a new computation when a Valid input is given and `bitString` is 0. The `bitString` register should be initialized to the input argument, and register `n` should hold the output. When the computation is finished, the `result` method should return a Valid result; while the computation is ongoing, `result` should return Invalid.

```minispec
typedef Bit#(32) Word;

module FindLongestBitRun;
    Reg#(Bool) initialized(False);
    Reg#(Bit#(6)) n(0);
    Reg#(Word) bitString(0);

    input Maybe#(Word) in default = Invalid;

    method Maybe#(Bit#(6)) result;
    endmethod

rule tick;
    if (isValid(in) && bitString == 0) begin
        n <= 0;
        bitString <= _____ [Part A2] ______;
        initialized <= True;
    end
    else if (initialized && (bitString != 0)) begin
        n <= n + 1;
        bitString <= ______ [Part A3] ______;
    end
endrule
endmodule
```

(A) (8 points) There are blanks in the code above labeled [Part A#]. #]. Fill in the missing code, by copying each of the lines below and filling in the blanks corresponding to parts A1, A2, and A3.

You may use any Minispec operators, built-in functions, and literals. You will not need additional registers to complete this problem. Do not add other rules, methods, or functions.

*(Label: 4A_1) A1: return (initialized & bitString == 0) ? _____: _____;

*(Label: 4A_2) A2: bitString <= ____________________________;

*(Label: 4A_3) A3: bitString <= ____________________________;
(B) (8 points) At cycle 0, the input is set to \texttt{Valid(32'b0111)}. **Copy and fill in the table below to indicate the values at the output of the `result()` method, the value in register \texttt{n}, and the value in the \texttt{bitString} register.** Write “Invalid” if a value is invalid, “?” if a value is unknown, and just a number to indicate a valid value (i.e. you do not need to write “Valid(5)”; just write “5”). “0b” indicates that the number after it is a binary value.

\textbf{(Label: 4B) Copy and fill in the table below}

<table>
<thead>
<tr>
<th>Cycle</th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input</td>
<td>0b0111</td>
<td>Invalid</td>
<td>0b1111</td>
<td>Invalid</td>
<td>0b0001</td>
<td>Invalid</td>
<td>Invalid</td>
</tr>
<tr>
<td><code>result()</code> output</td>
<td></td>
<td></td>
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<td></td>
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<td></td>
</tr>
<tr>
<td>value in register \texttt{n}</td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>value in \texttt{bitString}</td>
<td></td>
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<td></td>
<td></td>
</tr>
</tbody>
</table>