

6.004 Tutorial Problems

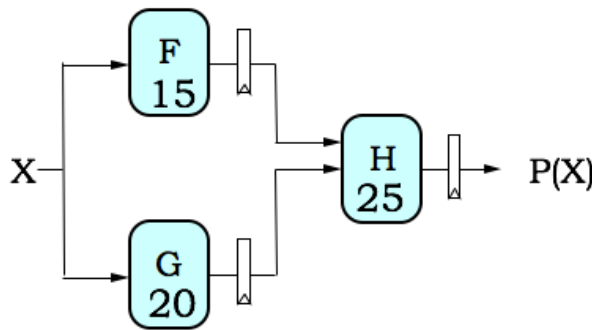
L12 – Introduction to Pipelining

Latency: the delay from when an input is established until the output associated with the input becomes valid.

- Combinational circuits: $L = t_{PD}$
- K-pipeline: $L = K * t_{CLK}$

Throughput: the rate at which inputs or outputs are processed.

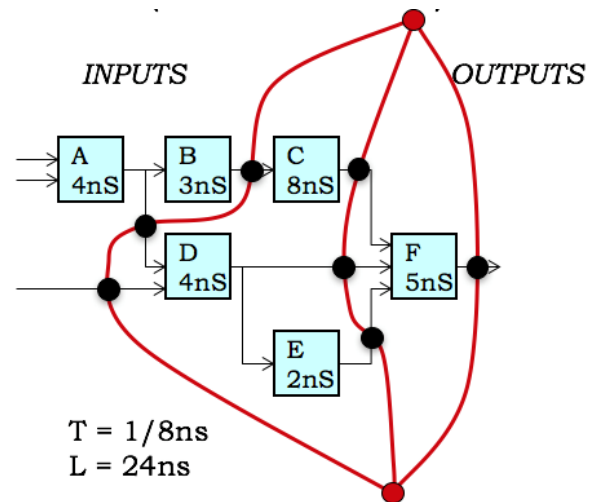
- Combinational circuits: $T = 1/L$
- K-pipeline: $T = 1/t_{CLK}$



Unpipelined:
 $L = 45\text{ns}$, $T = 1/L = 1/(45\text{ns})$
 2-stage pipeline [$t_{CLK}=25\text{ns}$]:
 $L = 2 * 25 = 50\text{ ns}$, $T = 1/(25\text{ns})$

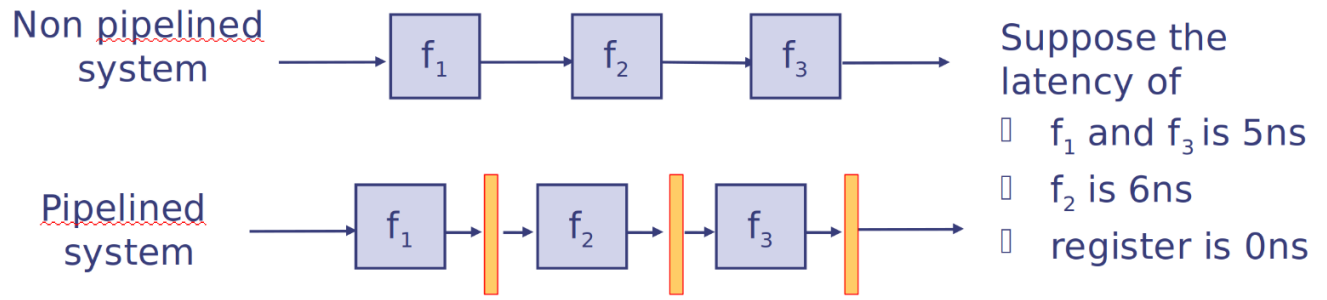
Pipelining methodology:

- Form 1-pipeline by adding registers to all outputs
- To add a pipeline stage, draw contour across all paths from inputs to outputs such that it doesn't cross other contours and all input-output paths cross the contour in the same direction. This ensures the pipeline is well-formed (same # of registers on all input-output paths). A K-pipeline has K registers on all input-output paths.
- Contours must take into account pipelined components.



		Clock cycle →			
		i	i+1	i+2	i+3
Pipeline stages ↓	F & G	F(X _i) G(X _i)	F(X _{i+1}) G(X _{i+1})	F(X _{i+2}) G(X _{i+2})	...
	H		H(X _i)	H(X _{i+1})	H(X _{i+2})

Pipelining trades improved Clock Period and Throughput for worse Latency. Consider the example shown below:



	Non pipelined	Pipelined
Clock period (ns)	$5+6+5=16$	6
Throughput (1/ns)	1/16	1/6
Latency (ns)	16	$3*6 = 18$

Problem 1. ★

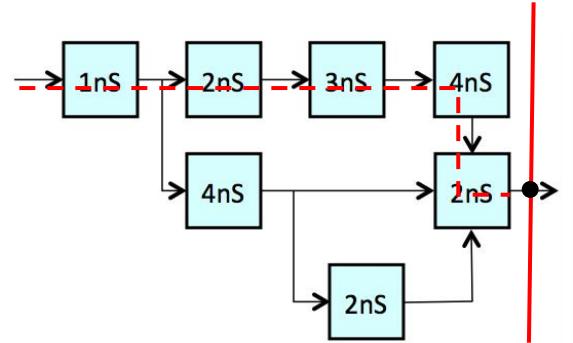
A simple combinational circuit is to be pipelined for **maximum throughput using a minimal number of registers**. For each of the questions below, please create a valid K-stage pipeline. **Show your pipelining contours** and place black circles (●) on the signal arrows to **indicate the placement of ideal pipeline registers** ($t_{PD}=0$, $t_{SETUP}=0$). Give the latency and throughput for each design. Remember that our convention is to place a pipeline register on each output.

- (A) (1 point). Show the maximum-throughput 1-stage pipeline.

Latency (ns): 12

Throughput (ns⁻¹): 1/12

As is our convention, there is a pipeline register on the output. The entire circuit is one stage so we don't add any other registers. The longest path is indicated in with a dashed line. It has latency 12ns, and the throughput is its reciprocal.

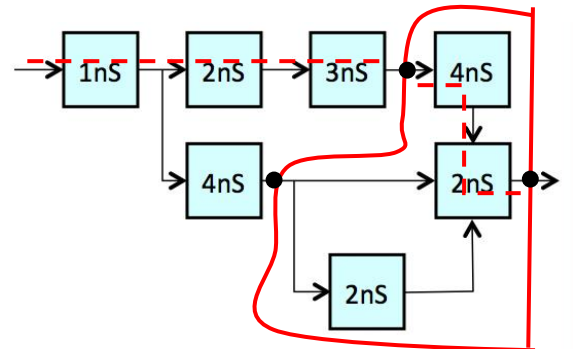


- (B) (2 points). Show the maximum-throughput 2-stage pipeline using a minimal number of registers.

Latency (ns): 2*6 = 12

Throughput (ns⁻¹): 1/6

Both stages have latency 6ns, which is the best possible, since the total latency is still at least 12ns. So the clock period is 6ns and the throughput is 1/6ns.

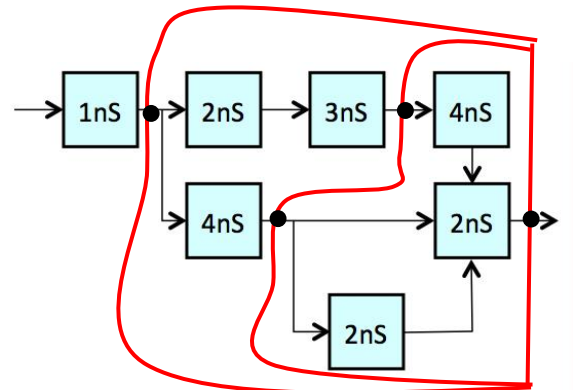


- (C) (2 points). Show the maximum-throughput 3-stage pipeline using a minimal number of registers.

Latency (ns): 3*6 = 18

Throughput (ns⁻¹): 1/6

There is no way to improve the throughput over the 2-stage pipeline. You can see this by considering the critical path: if you wanted a throughput of more than 1/6, each stage latency would have to be <6ns. But you can only fit the 1ns and 2ns components in the first stage, the 3ns component in the second stage, and then the 4ns component in the third stage, so it's impossible. So our 3-stage pipeline still has throughput 1/6ns. To use a minimal number of registers, we just add one register to our 2-stage pipeline; other answers are possible.



(D) (2 points). Show the maximum-throughput 4-stage pipeline using a minimal number of registers.

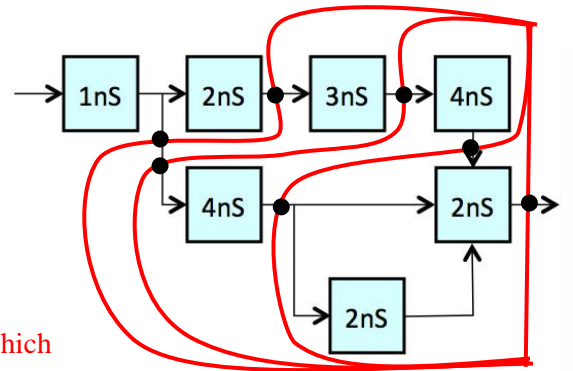
Latency (ns): $4 * 4 = 16$

Throughput (ns⁻¹): $1/4$

The four stages have latency 3ns, 3ns, 4ns, and 4ns.

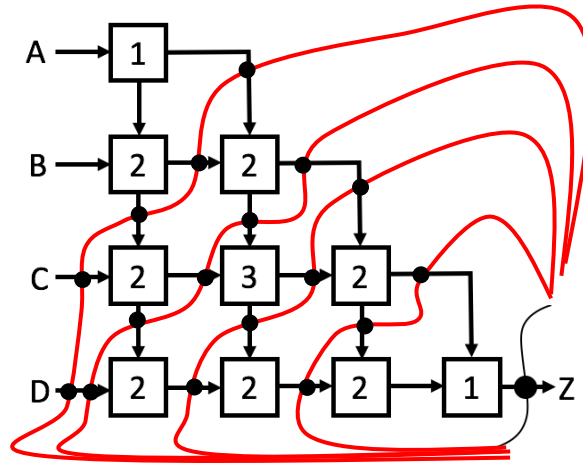
The latency is the number of stages times the clock period, which equals the maximum latency of one stage, or 4ns here.

The throughput is 1 over the clock period, or 1/4ns.



Problem 2.

The following 1-stage pipelined circuit computes Z from the four inputs A, B, C, and D. Each component is annotated with its propagation delay in ns.



- (A) Please pipeline the circuit above for maximum throughput with the minimum possible latency using ideal pipeline registers ($t_{PD} = 0$, $t_{SETUP} = 0$). Show the location of pipeline registers in the diagram above using filled-in circles, like the one shown on the Z output. Please give the latency and throughput of the resulting pipelined circuit.

Latency (ns)? 5*3 = 15

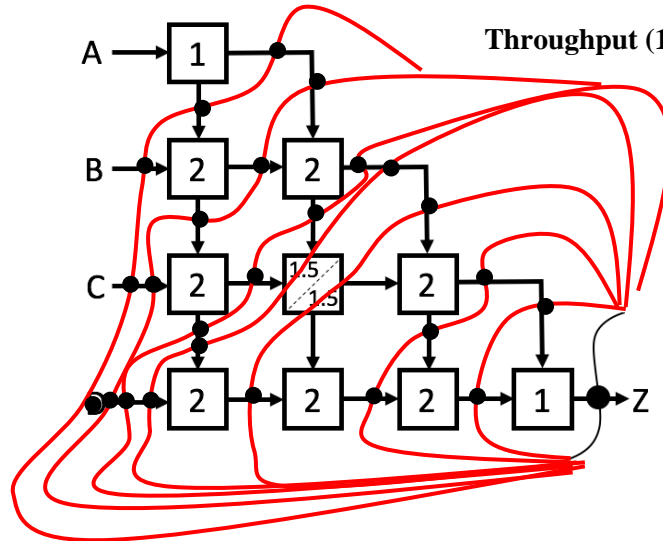
Throughput (1/ns)? 1/3

Since there's a component with latency 3, and each component must be wholly in one pipeline stage, there will always be a pipeline stage with latency at least 3ns. So the minimum clock period is 3ns and the maximum throughput is 1/3ns. This is achieved as above. Every pair of connected components with one output connected to another's input must be separated into different pipeline stages if the components' total latency is more than 3, which is almost every pair, only excluding the 2+1 and 1+2 at the start and end. We end up with 5 contours and 5 stages.

(B) Now suppose the “3” component is replaced by a 2-stage pipelined component with a minimum t_{CLK} of 1.5ns. Again, please pipeline the circuit below for maximum throughput with the minimum possible latency using ideal pipeline registers. Show the location of pipeline registers in the diagram below using filled-in circles, like the one shown on the Z output. Please give the latency and throughput of the resulting pipelined circuit.

Latency (ns)? 8*2 = 16

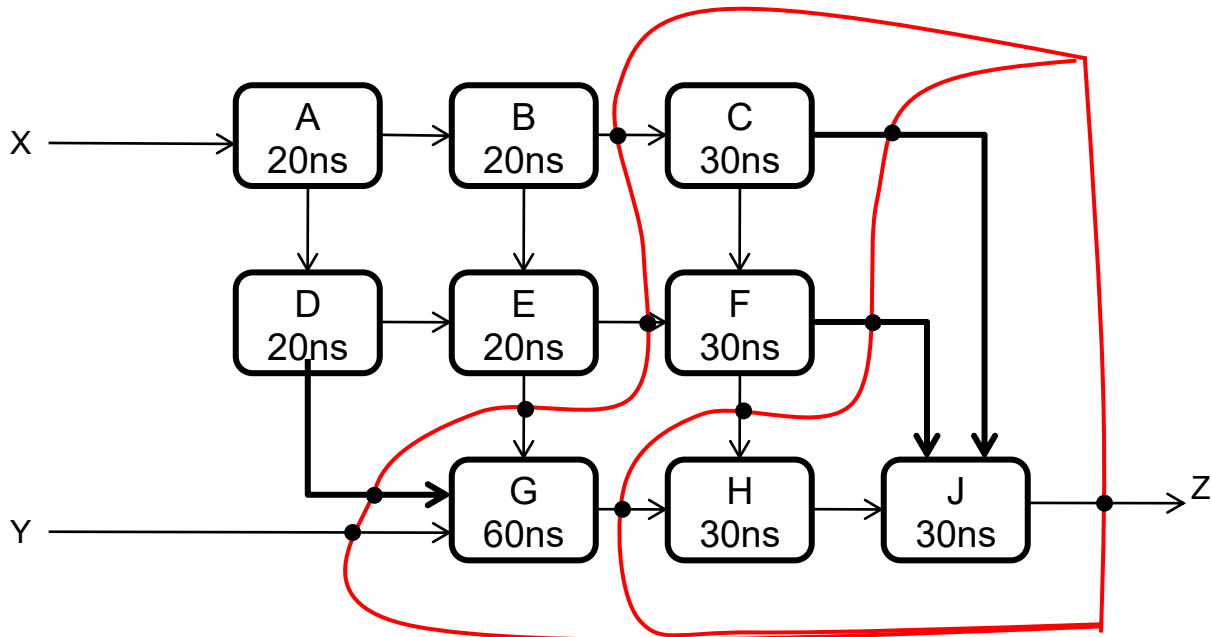
Throughput (1/ns)? 1/2



Now the maximum throughput is $1/2ns$, and every pair of connected components with one output connected to another's input must be separated into different pipeline stages. Note that we don't add registers to the new 2-stage pipelined component. We assume it comes with its own internal registers, 2 along every input-output path, for the purpose of ensuring every path goes through the same number of registers. We end up with 7 contours and 7 stages.

Problem 3.

An unidentified government agency has a design for a combinational device depicted below:



Although you don't know the function of each of the component modules, they are each combinational and marked with their respective propagation delays. You have been hired to analyze and improve the performance of this device.

(A) (1 Point) What are the throughput and latency for the unpipelined combinational device?

Latency: 180 ns; Throughput: 1/180 ns⁻¹
 The longest path is A → (B or D) → E → G → H → J, for 20+20+20+60+30+30ns

(B) (4 Points) Show how to pipeline the above circuit for maximum throughput, by marking locations in the diagram where registers are to be inserted. Use a minimum number of registers, but be sure to include one on the output. Assume that the registers have 0 t_{PD} and t_{SETUP}.

(mark register locations in diagram above)

Since G has the maximum latency of any component, 60ns, the maximum throughput is 1/60ns. It makes sense to draw contours right before and after G, and then in the right places so every stage has latency at most 60ns, and it turns out it works with three stages.

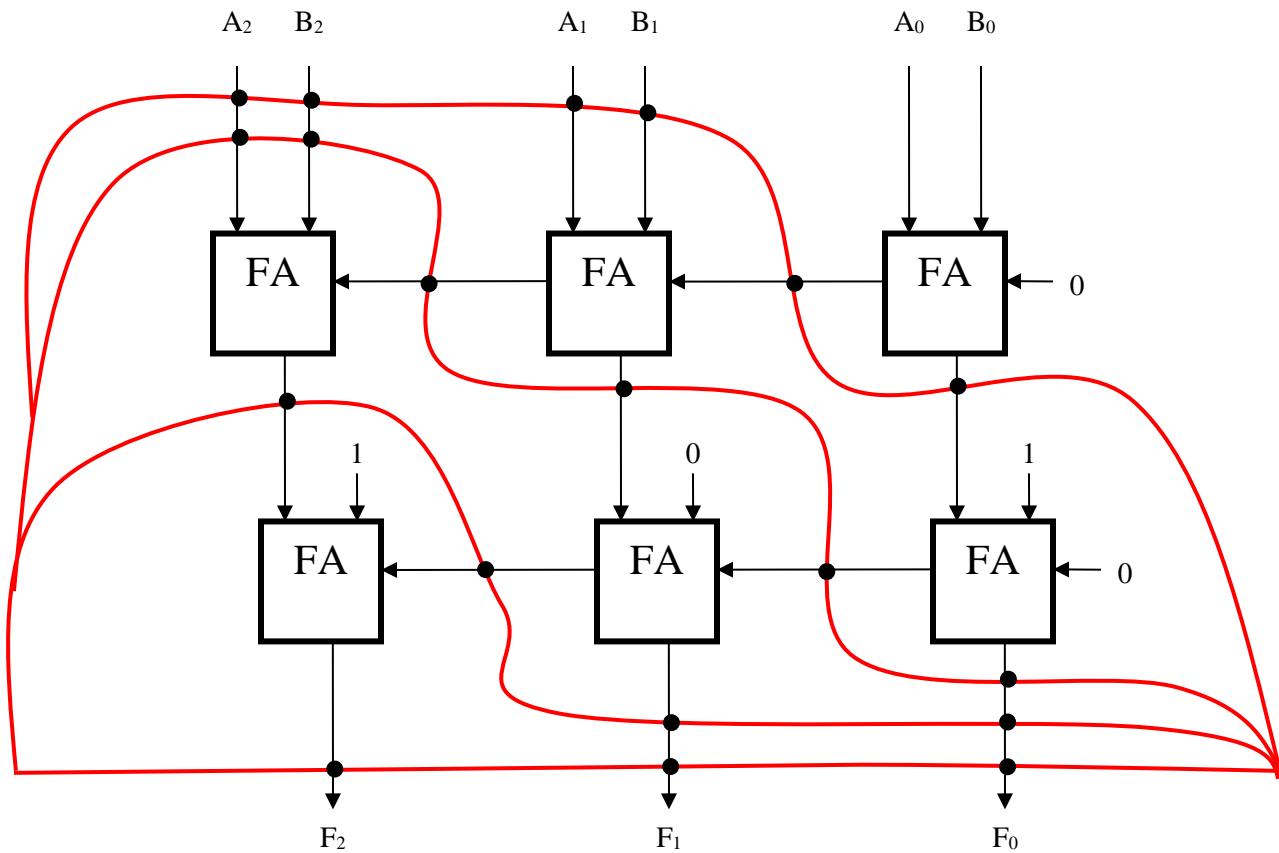
(C) (1 Point) What are the latency and throughput of your pipelined circuit?

Latency: 180 ns; Throughput: 1/60 ns⁻¹

Each stage has latency 60ns, so the clock period is 60ns. The pipelined circuit's latency is the number of stages times that, or 180 ns. The throughput is 1 over the clock period.

Problem 4. ★

The following circuit uses six full adder modules (as you've seen in lecture and lab) arranged in a combinational circuit that computes a 3-bit value $F=A+B+5$ for 3-bit inputs A and B :



The full adders have a t_{PD} of 6ns.

(A) Give the latency and throughput of the combinational circuit.

Latency: 24 ns; Throughput: 1/24

The longest paths go from A_0 or B_0 through 4 full adders to F_2 , so the latency is 4 * the full adders' propagation delay.

(B) Indicate, on the above diagram, appropriate locations to place ideal (zero-delay) registers to pipeline the circuit for *maximum throughput* using a *minimum number of registers*. Be sure to include a register on each output.

(mark circuit above)

As shown, we ensure no two connected full adders are in the same stage, and also that every input-output path goes through every contour.

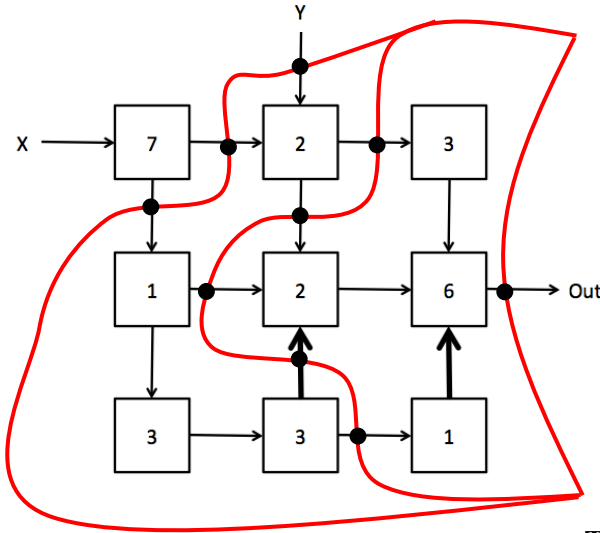
(C) Give the latency and throughput of your pipelined circuit.

Latency: 24 ns; Throughput: 1/6

Clock cycle is 6ns

Problem 5. ★

(A) You are provided with the circuit shown below. Each box represents some combinational logic. The number in each box is the t_{PD} of that combinational logic. The circuit has two inputs, X and Y, and one output Out. Pay close attention to the direction of the arrows especially the arrows shown in **bold**. What is the latency and throughput of this combinational circuit?



Latency (ns): 22

Throughput (1/ns): 1/22

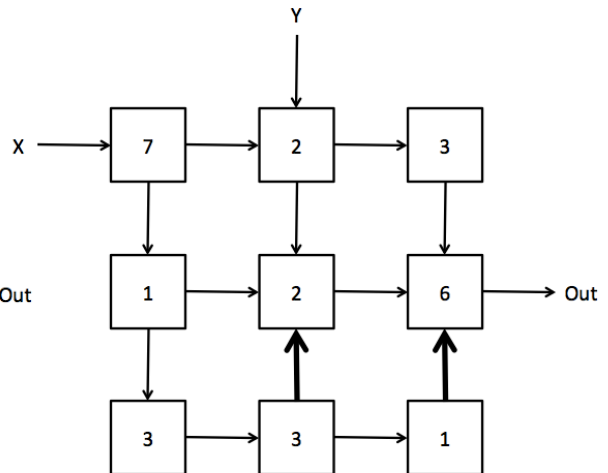
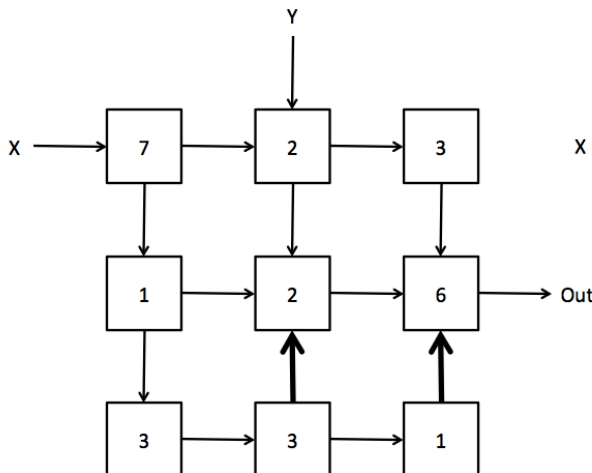
Longest path is $7 \rightarrow 1 \rightarrow 3 \rightarrow 3 \rightarrow 2 \rightarrow 6$

(B) Draw contours through the circuit above to produce a valid pipelined circuit whose $t_{CLK} = 9ns$ with minimum latency. Extra copies of the diagram are included below. Please use a large dot to indicate the location of each pipeline register. Assume that you have ideal pipeline registers ($t_{PD}=t_{CD}=t_{Setup}=t_{Hold}=0$ ns). Pay close attention to the direction of each arrow to ensure that you produce a valid pipeline. What is the latency and throughput of this pipelined circuit?

Latency (ns): 27

Throughput (1/ns): 1/9

3 pipeline stages

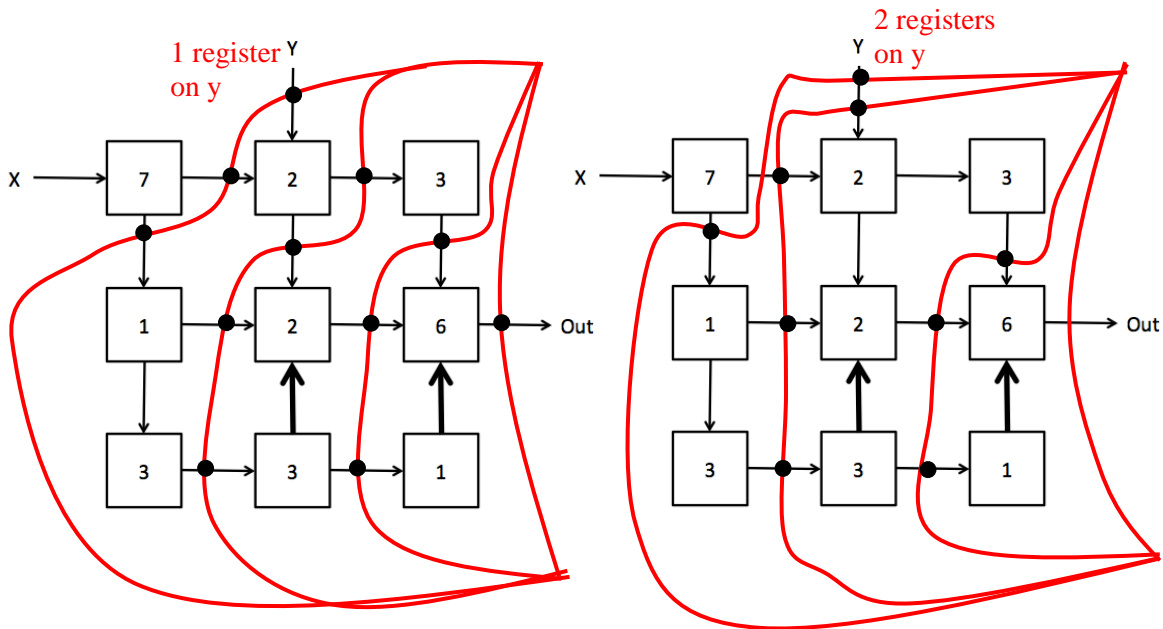


- (C) You are now asked to consider the performance of this circuit using different clock periods while achieving the minimum latency. For each suggested t_{CLK} , specify whether or not you can create a **valid** pipelined circuit using that clock period. If you can, then provide the latency and throughput of the resulting circuit and specify the number of registers at each input. If it results in an invalid pipeline, enter NA for the rest of the row.

Extra copies of the circuit diagram are provided below.

t_{CLK}	Valid/Invalid	Latency (ns)	Throughput (1/ns)	Pipeline registers at input X	Pipeline registers at input Y
6 ns	Invalid	NA	NA	NA	NA
7 ns	Valid	28	1/7	0	1 or 2

With one component of latency 7ns, a clock period of 6ns is not possible. There are several possible solutions for a clock period of 7ns.



Problem 6.

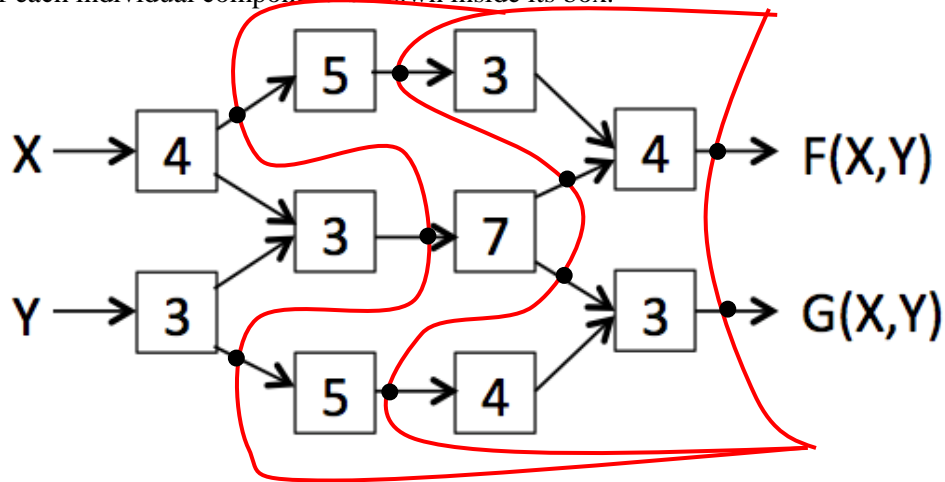
A complex combinational circuit is constructed entirely from 2-input NAND gates having a propagation delay of 1 ns. If this circuit is pipelined for maximal throughput by adding (non-ideal) registers whose setup time and propagation delay are each 1 ns, what is the throughput of the resulting pipeline? Enter a number, a formula, or “CAN’T TELL”.

$$t_{CLK} \geq t_{PD,R} + t_{PD, NAND} + t_{setup, R} \\ = 1 + 1 + 1 = 3$$

Throughput (ns^{-1}): 1/3

Problem 7.

The following combinational circuit computes $F(X,Y)$ and $G(X,Y)$ from inputs X and Y . The t_{PD} (in ns) of each individual component is shown inside its box.



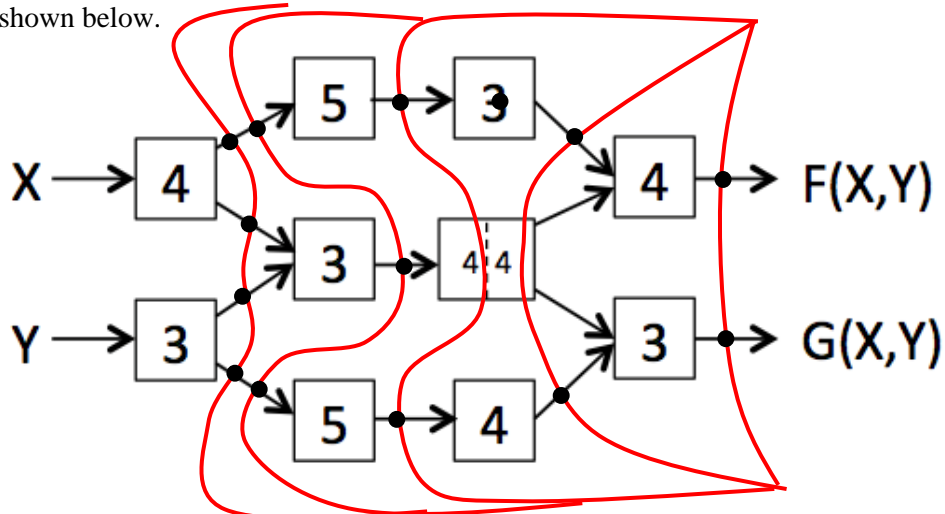
- (A) Using ideal zero-delay registers, mark the location of the minimal number of registers necessary to achieve maximum throughput. Give the latency and throughput of your pipelined circuit.

mark diagram above

Latency: 21 (ns); Throughput: 1/7 (1/ns)

The clock period again is at least 7ns, the maximum latency of one component. 4 stages works.

Rummaging through the stockroom you find a pipelined component with two pipeline stages that can replace the “7” module. The minimum t_{CLK} for the new component is 4ns. The updated circuit is shown below.



- (B) Using ideal zero-delay registers, mark the location of the minimal number of registers necessary to achieve maximum throughput. Give the latency and throughput of your pipelined circuit.

mark diagram above

Latency: 25 (ns); Throughput: 1/5 (1/ns)

Now the maximum clock period is 5ns and 5 stages works.